České vysoké učení technické v Praze
Fakulta jaderná a fyzikálně inženýrská
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Diplomová práce

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Mikroprocesorem řízené rozhraní USB pro detektor Medipix2

Diplomová práce

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Czech Technical University in Prague
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Microprocessor controlled USB interface for Medipix2 detector

Diploma Thesis

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Academic year: **2004/2005**

Prohlašuji, že jsem předloženou práci vypracoval samostatně a že jsem uvedl veškerou použitou literaturu.

Praha, 10.5.2005 Zdeněk Vykydal

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Abstrakt

Cílem této diplomové práce je návrh, sestavení a oživení rozhraní pro detektor Medipix2[1] využívající sběrnice USB[2].

Hybridní polohově citlivý detektor Medipix2 je sestaven ze dvou částí. První z nich je křemíkový senzor, který je rozdělen na matici 256 x 256 čtvercových buněk o hraně 55 μm. Druhou část tvoří čip, který pro každou buňku senzoru obsahuje zesilovač, dva diskriminátory a 13-bitový čítač. Řízení akvizice a čtení dat z detektoru Medipix2 bylo dosud možné pouze prostřednictvím rozhraní (MUROS2[3]), které tvoří most mezi detektorem a řídícím počítačem vybaveným speciální kartou. Při měření prostřednictvím tohoto rozhraní je navíc třeba použít externí zdroje napětí. Vzhledem k velkým rozměrům všech těchto zařízení a limitované délce kabeláže byly možnosti využití detektoru omezené.

V případě nového rozhraní bylo cílem výše uvedené nevýhody eliminovat. Proto je veškerá elektronika potřebná pro měření s detektorem Medipix2 integrována na jediné desce plošného spoje o rozměrech 60 x 45 mm^2. Veškerá potřebná napájecí napětí, včetně zdroje vysokého napětí pro senzor detektoru (do 90 V), jsou odvozena přímo z USB sběrnice. Toto nové rozhraní je navíc řízeno mikroprocesorem, který umožňuje velkou flexibilitu měření a další rozšiřování zařízení.

[1] MEDical Imaging PIXel detector of 2nd generation
[2] Universal Serial Bus
[3] Medipix2 re-Usable Read-Out System version 2

Abstract

This diploma thesis is devoted to the development of the new USB[1] based read-out interface for the Medipix2[2] detector.

The hybrid silicon pixel detector device Medipix2 consists of a sensor chip with 256 x 256 square pixels of 55 μm size each and a read-out chip containing an amplifier, two discriminators and a 13-bit counter for each pixel. Up to this day the Medipix2 device had been connected to a PC equipped with a DAQ card via devoted interface (MUROS2[3]). In addition, external power supplies were needed. Due to the large dimensions of these external devices and limited lengths of cabling, the operability and uses of the detector become reduced.

With the new interface the many drawbacks and limitations are eliminated. All necessary detector support is integrated into one compact device (60 x 45 mm^2). All power supplies including detector bias (up to 90 V) are internally derived from the voltage provided by the USB connection. The new interface is controlled by microprocessor providing high level of flexibility.

[1] Universal Serial Bus
[2] MEDical Imaging PIXel detector of 2nd generation
[3] Medipix2 re-Usable Read-Out System version 2

Introduction

Significant technological progress in the last years in electronics opens up new possibilities in particle detection and imaging. Nowadays promising digital detector systems such as Medipix2 (MEDical Imaging PIXel detector of 2nd generation) [1] are available making possible real time imaging with high sensitivity and broad dynamic range. The range of applicability of these imaging systems goes from various medical applications (digital mammography, dental X-ray diagnostics, DNA studies, small animal imaging, etc.) up to non destructive material studies.

The hybrid pixel detector device Medipix2 consists of a semiconductor sensor chip with 256 x 256 square pixels of 55 μm size and a ASIC[1] read-out chip containing the amplifier, two discriminators (high and low threshold) and 13-bit counter for each pixel. Every cell is working as a single photon counting device for photons with energy given by low and high threshold settings. This hybrid configuration offers to optimize the read-out electronics and sensor separately. This brings flexibility in the choice of the read-out chip design technology. In addition, suitable sensor material can be chosen with respect to the specific application.

Currently, the acquisition controlling and data reading can be realized only via devoted interface MUROS2 (Medipix2 re-Usable Read-Out System version 2). MUROS2 is the FPGA[2] based device as a bridge between Medipix2 chipboard (which can contain up to eight Medipix2 chips) and a universal data acquisition card (National Instruments DIO-653X) for PCI[3] computer slot. External power supplies for Muros2 interface and detector bias are needed. Due to large dimensions of these external devices and limited lengths of cables the applicability of the detector is restricted.

The subject of my work is to design and realize an alternative, microprocessor controlled, interface for Medipix2 system. In the past years, the USB[4] interface has become a widespread interface standard not only in desktop computers but also in

[1] Application Specific Integrated Circuit
[2] Field Programmable Gate Array
[3] Personal Computer Interconnected
[4] Universal Serial Bus

various portable devices. To extend the applicability of the Medipix2 device and make it more portable, the USB interface was chosen. The work carried out can be divided into three main tasks:

- to design, construct and put into operation the interface hardware,
- to develop and debug software for microcontroller,
- to develop software for control PC[5].

My job has been the realization of the first two tasks of this work. Developing the software for control PC is proceeding in our team within a complex program package, which will enable measurements with both interfaces, stepper motors controlling (sample movement, rotation...), etc.

[5] Personal Computer

1 Position Sensitive Semiconductor Detectors

In this chapter I briefly summarize the basic information about semiconductor detectors (spectroscopic and position sensitive) as well as reviewing the principle of detection of ionizing radiation with this type of detector. Later in this chapter the detailed description of the Medipix2 detector (without the functions which are not supported by current chipboard) will be given.

1.1 Semiconductor detectors [2]

The most widely used detectors of this type today are based on silicon or germanium[1]. The reason is that these materials are, due to extensive research in semiconductor junctions as electronics components, well explored and also the production technology of pure monocrystals is well known. The basic characteristics of pure (intrinsic) silicon and germanium are shown in Table 1.1.

Silicon (Z = 14) is usually used for heavy charged particle (protons, α particles...) and low energy photon detectors. The advantage of silicon is wide energy gap and relatively high resistivity even at room temperature.

Germanium with atomic number Z = 32 can be advantageously used for high energy photon detection. Technology of producing large and high purity germanium monocrystals is widely developed at present. From the properties listed in Table 1.1 results the necessity of cooling germanium detectors to increase the resistance of the crystal and decrease the thermal current and noise. Commonly liquid nitrogen (T = 77 K) cooling is used.

[1] Usage of the novel high Z detector materials like GaAs, CdTe, HgI, etc. is still rare

Intrinsic semiconductor	**Si**	**Ge**
Atomic number Z	14	32
Mass number A	28,09	72,60
Density $(300K)$ $[kg.m^{-3}]$	2330	5330
Atomic density $[m^{-3}]$	$4{,}96.10^{28}$	$4{,}41.10^{28}$
Relative dielectric constant	12	16
Energy gap E_g $(300K)$ $[eV]$	1,115	0,665
Energy gap E_g $(77K)$ $[eV]$	1,154	0,730
Electron density n_i $(300K)$ $[m^{-3}]$	$1{,}5.10^{16}$	$2{,}4.10^{19}$
Intrinsic electric resistivity r_i $(300K)$ $[\Omega m]$	$2{,}3.10^{3}$	0,47
Electron mobility μ_e $(300K)$ $[m^2V^{-1}s^{-1}]$	0,135	0,39
Hole mobility μ_d $(300K)$ $[m^2V^{-1}s^{-1}]$	0,048	0,19
Electron mobility μ_e $(77K)$ $[m^2V^{-1}s^{-1}]$	2,1	3,6
Hole mobility μ_d $(77K)$ $[m^2V^{-1}s^{-1}]$	1,1	4,2
Energy for electron-hole pair generation w $(300K)$ $[eV]$	3,62	-
Energy for electron-hole pair generation w $(77K)$ $[eV]$	3,76	2,96
Fano factor F $(77K)$	0,084 - 0,143	0,058 - 0,129

Table 1.1: *Characteristics of intrinsic silicon and germanium*

As consequence of high thermal stimulated current[2], which for a silicon plate of 1 cm^2 area becomes about four orders of magnitude greater than the effective signal[3], is it not possible to use an intrinsic semiconductor as a radiation detector. For germanium the situation is even about several orders of magnitude worse. The only known and viable method enabling an effective decrease of thermal stimulated current of semiconductor detectors is using the properties of the P-N junction.

1.1.1 Doped semiconductors

Silicon and germanium belong to group IV of the periodic table of elements. Both materials crystallize in a cubic crystal structure where their four valence electrons mediate covalent bonds between nearby atoms. In such a crystal at non-zero temperature, part of its thermal energy is given to the electrons. This energy can be large enough to allow valence electrons to overcome the energy gap from valence to the conduction band. Thus electron-hole pairs are created which, as charge carriers, can move in the crystal by application of an external electric field causing the thermal electric current.

If the crystal contains a small concentration (relatively less than 10^{-6}) of elements from V. group of periodic table of elements, there atoms can replace the semiconductor atoms at some places. Four out of five donor valence electrons mediate the covalent bonds with surrounding atoms. The remaining fifth electron is only weakly bonded to the atom of impurity and needs only a small amount of energy to reach the conduction band. However in this case, no corresponding hole is created! This small energy is with high probability obtained by thermal excitation. Because the density of impurities is in most cases much larger than concentration of thermal excited intrinsic electrons, almost all electrons in conduction band comes from ionized donors. Larger then intrinsic electron density in conduction band increases the recombination speed and as a result

[2] For silicon plate of d = 1mm thickness, and bias voltage U = 10V is the current density of thermal stimulated current $i_0 \geq 10^{-3}$Acm^{-2} ([2], p.141)

[3] Mean value of the signal current is for the same plate (Si, d = 1mm, U = 10V) about 5.10^{-7}A ([2], p.141)

the balance of electron and holes densities is altered. As a consequence, the electron density in the conduction band exceeds the hole density in the valence band by several orders of magnitude. As the majority charge carriers are electrons and minority holes, this type of doped semiconductor is called N-type semiconductor.

On the contrary, P-type semiconductors are doped by atoms from group III of the periodic table of elements (acceptors). Atoms of trivalent impurities are to the atoms of the medium bounded only by three instead of four covalent bonds. The fourth, unsaturated atomic bond represents a hole with similar parameters as the temperature induced hole carriers. These acceptor vacancies are occupied by temperature excited electrons from the conduction band after which the positive charged holes remain in the valence band. This again leads to an unbalance of charge carriers when the hole density in the valence band is much greater than the electron density in the conduction band.

1.1.2 P-N junction

A P-N junction is forming by changing the type and concentration of impurities along the crystal (e.g. by diffusion of acceptors on the wafer of N-type semiconductor). Suppose sufficient temperature, so that all dopes in semiconductor are ionized. At the P-type semiconductor the concentration of the holes predominates electron concentration by several orders, while at N-type semiconductor the situation is reversed. At the junction area, the gradient of concentration of charge carriers causes the diffusion of holes to the N-type region and electrons to the P-type side. For that reason, at the junction area is the lack of movable charge carriers, but there are still unmovable ionized donors and acceptors, fixed in crystal lattice. As a result, the electric field of high intensity in direction of potential drop arises. This field affects against the charge carriers diffusion until the current density caused by the diffusion is compensated by drift current density and the equilibrium was established.

If we have the intention to use P-N junction for ionizing radiation detection, it is necessary to polarize it in so-called reverse direction. In this case, the positive polarity of applied voltage is on N-type side and negative polarity is on P-type region. In this way applied voltage causes expansion of depleted area (area without movable charge carriers) suitable for detection. Electron-hole pairs formed in depleted area by ionizing radiation interaction than create the current (respectively charge) signal, which can be amplified and measured. Through the reverse polarized P-N junction only minority carrier current flows. If we achieve, that this reverse current will be several times less than the signal current, than the reverse polarized P-N junction will have the character of spectrometric detector with sensitive volume of depleted area size.

1.2 Position sensitive detectors [3]

The development of the new detectors lies in the domain of high energy physics and related fields. At new colliders such as the LHC (Large Hadron Collider) at CERN[4], new detectors are required for monitoring the tracks of primary and secondary particles produced by colliding particle beams. The task of tracking detectors is to resolve the

[4] Centre Europeen pour Recherche Nucleare

various particle tracks and to assign them to primary or secondary vertices. For this purpose several types of position sensitive detectors have been developed.

First of all are the **microstrip detectors**. These devices consist of thin (usually about 300 μm thick), high resistivity silicon sensors segmented into narrow strips with pitch in the order of tens of microns. Reverse biased P-N junctions structures, formed between strips and the rear side of the detector, determine one dimensional coordinate of the crossing particles. The charge generated from individual events is spread between nearby strips due to drift and diffusion. With analog read-out electronics, the centre of the charge distribution can be calculated. It this manner it has been possible to reach excellent spatial resolution down to 5 μm [6]. The major setback of this type of detector is that multiple tracks cannot be resolved unambiguously.

Advances in CMOS[5] technology (1 μm[6] CMOS technology became standard in the early 90s) enabled to construct two-dimensional matrices of P-N junctions (diodes) at micrometer scale. Further improvement in CMOS technology enabled the possibility of integrating the read-out logic unit close to the detector elements. Following the nomenclature used for CCDs[7] and optical devices the term **pixel detector** is used for such devices. Each detecting element from the matrix is composed of one diode attached to its read-out electronics (with dimensions equal to the detection element). The concept of active pixel detectors consists in having the electronics cell equally dimensioned and close to the corresponding pixel. Thanks to the proximity between the detection and read-out parts of the device, the capacitance of the collection electrode can remain very small and the signal to noise ratio high. Further, it is also possible to implement a number of important logical features such as data selection (zero-suppression). Several possibilities of realizing pixel detectors have been developed.

In **monolithic pixel detectors** (see Figure 1.1) electronics circuitry is integrated with the detecting elements onto the same substrate. This results in a more robust and thinner device (reducing energy loss and scattering inside a complex high energy particle detector) compared to the hybrid approach (see below).

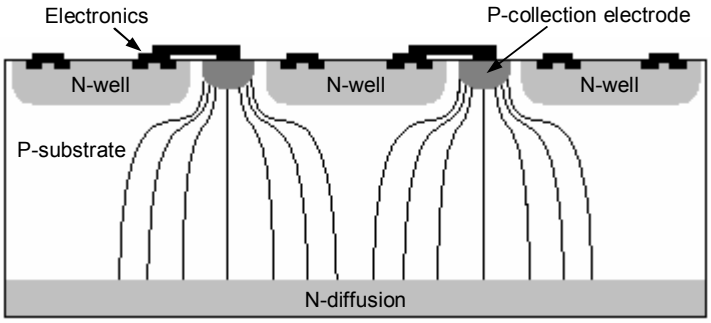


Figure 1.1: *Cross sectional view of a part of monolithic pixel detector*

A different processing technique is called SOI (Silicon On Insulator). An insulating layer separates the active detector part from the read-out electronics which are

[5] Complementary Metal Oxide Semiconductor
[6] 1 μm corresponds to the transistor gate length and is a measure for the electronics component miniaturization
[7] Charge Coupled Device

embedded in a thin silicon layer (see Figure 1.2). The high resistivity substrate below the oxide layer may be used as the detection volume. This reduces the drain and source diode capacitance making the electronics faster for a given power consumption. Another advantage of SOI detectors is radiation tolerance. The drawback of this technology is that design requires nonstandard processing (double-sided processing, P-implants underneath the oxide layer of the SOI wafer) which expensive manufacturing costs.

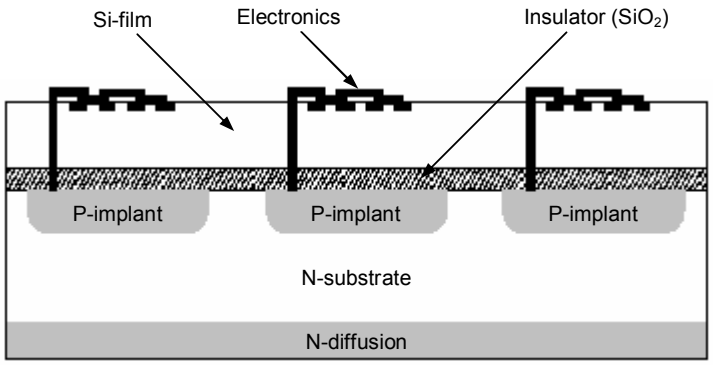


Figure 1.2: *Cross sectional view of a segment of a pixel detector in SOI technology*

In a **hybrid pixel detector** the read-out chip and the sensor are manufactured separately. Each of the two parts of the detector have a matching matrix of spot electrodes which are connected together mechanically and electrically through small connecting spherical bonds (usually made out of solder or indium with diameter of about 20 μm) as depicted in Figure 1.3. This procedure is called bump-bonding process and offers the possibility of optimizing the read-out electronics and the sensor independently. The possibility of choosing the sensor material makes this approach highly attractive in medical imaging applications. GaAs or CdTe can be used instead of silicon which, being a low-Z material, has low absorption efficiency for X-rays with energies greater than about 20 keV [6]. It is important to note that only the hybrid approach allows the design of the pixel read-out in standard CMOS technology which is a major consideration in view of processing costs.

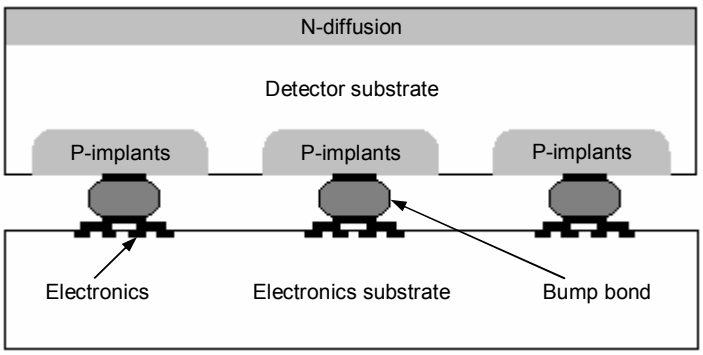


Figure 1.3: *Cross section through a part of a hybrid pixel detector*

This thesis concentrates on the Medipix2 pixel imaging chip which is designed as a hybrid in standard CMOS technology.

1.3 Medipix2 detector [9]

The hybrid pixel detector Medipix2 (see illustration in Figure 1.5) is the successor of the Medipix1 photon counting chip. Fast progress of CMOS technology enabled enhanced functionality of the pixel cell while at the same time providing a significant reduction in pixel size. The square pixel size of 55 µm side length overcomes one of the limitations of the Medipix1 chip and makes the Medipix2 chip competitive with most of the existing imaging devices in terms of spatial resolution. The chip is designed and manufactured in six-metal 0.25 µm CMOS technology. Direct X-ray conversion in a semiconductor sensor minimizes image blurring and avoids the additional step of converting X-rays into visible light.

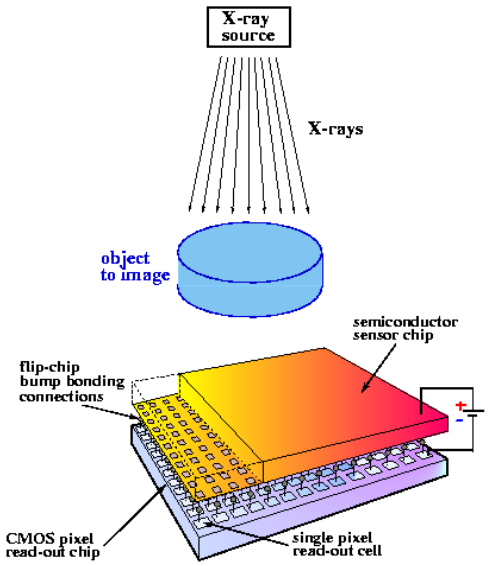


Figure 1.5: *Medipix2 detector and imaging function illustration [1]*

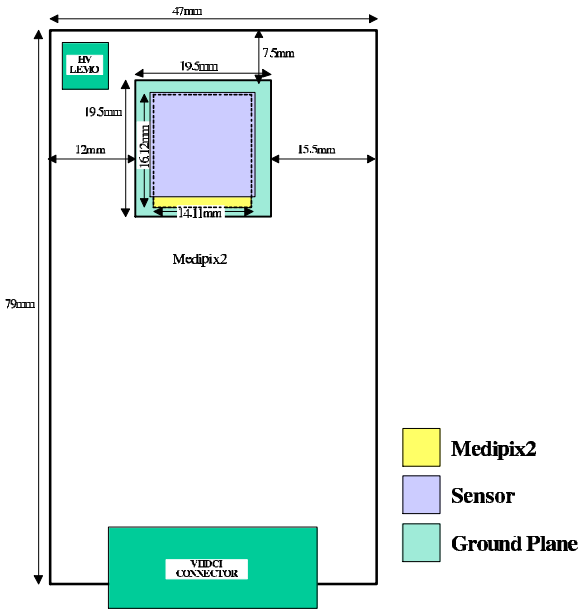


Figure 1.5: *Medipix2 chipboard*

1.3.1 Medipix2 chipboard specifications

Medipix2 chips are currently available on chipboards as shown in Figure 1.5 (with dimensions 47 x 79 mm^2). The Medipix2 chip is situated in the middle upper side of the board. In the upper left corner is the LEMO connector (type EPL.00.250.NTN) for detector bias voltage. The chipboard is connected via 68-pin VHDCI[8] connector to the read-out electronics. Description of the pin connections of this connector is given in Table 1.2 and Table 1.3. The complete chipboard scheme can be found in Appendix A.1. There is a new chipboard in production which is smaller (43 x 58 mm^2) and also supports some new features such as I^{2}C bus[9] controlled temperature monitoring and EEPROM[10] for configuration storage (see Appendix A.2).

[8] Very High Density Cable Interconnect
[9] Internal Integrated Circuit bus
[10] Electrically Erasable Programmable Read Only Memory

DIGITAL PINS				
Pin		**I/O**[11]	**Signal type**	**Description**
Name	**Num**			
PENABLE_IN[12]	2	I	LVDS	Falling edge starts operation if RESET and SHUTTER aren't active (High)
NENABLE_IN[13]	36	I	LVDS	Falling edge starts operation if RESET and SHUTTER aren't active (High)
PENABLE_OUT	34	O	LVDS	High: Any operation can be performed Low: End of operation
NENABLE_OUT	68	O	LVDS	High: Any operation can be performed Low: End of operation
PFCLK_IN	3	I	LVDS	Fast Clock input
NFCLK_IN	37	I	LVDS	Fast Clock input
PFCLK_OUT	33	O	LVDS	Fast Clock output
NFCLK_OUT	67	O	LVDS	Fast Clock output
PDATA_IN	4	I	LVDS	Serial data input
NDATA_IN	38	I	LVDS	Serial data input
PDATA_OUT	32	O	LVDS	Serial data output
NDATA_OUT	66	O	LVDS	Serial data output
RESET	60	I	CMOS	High: Any IO operation or counting can be done Low: Resets the chip IO counters and FSR
SHUTTER	26	I	CMOS	High: Any IO operation can be done Low: Chip is in counting mode (RESET is High)
M0	61	I	CMOS	Operation select bit 0
M1	27	I	CMOS	Operation select bit 1
P_S	59	I	CMOS	High: Parallel readout (not supported) Low: Serial readout
SPARE_FSR	25	I	CMOS	Selects a FSR[14] row to be used
POLARITY	58	I	CMOS	High: Pixel is set to collect positive charges (holes) Low: Pixel is set to collect neg. charges (electrons)
ENABLE_TPULSE	10	I	CMOS	High: Enables the pixel test Low: Disables the pixel test
ENABLE_CST	43	I	CMOS	High: Enables the CST[15] (not supported) Low: Disables the CST
CST_TG_OUT	9	O	CMOS-HiZ	Trigger output from 9 CST pixels
ANIN_A1	57	I	CMOS	Select analog input for the pixel test
SCL_I2C	64	I	CMOS	I^2C serial bus clock input
SDA_I2C	65	I/O	CMOS	I^2C serial bus data input/output
ANALOG PINS				
EXTDAC_IN	45	I	Analog	External DAC input to set any of the 14 DACs
ANIN_N02	46	I	Analog	Pixel test voltage input 1
ANIN_N04	47	I	Analog	Pixel test voltage input 2
DAC_OUT	7	O	Analog	Analog buffered output to measure one of the 14 DACs
DAC_BIAS	11	I	Analog	Sets the Bias reference voltage to the chip. Default value is 1,384V

Table 1.2: *Chipboard digital and analog pinout*

[11] I = input, O = Output
[12] P: Positive LVDS (Low Voltage Differential Signaling) signal
[13] N: Negative LVDS signal
[14] Fast Shift Register
[15] Charge Sharing Test

POWER SUPPLIES					
Pin		I/O	Signal type	Voltage	Description
Name	Num				
VDD	<50:53>	I	Analog	+2,2 V	Digital positive supply
VDDA	48,49	I	Analog	+2,2 V	Analog positive supply
VDDLVDS	<54:56>	I	Analog	+2,2 V	LVDS positive supply
VDD_BIAS	44	I	Analog	+2,2 V	Supply for DAC_BIAS mirroring
VCC	35	I	Analog	+5 V	MAX4634 positive supply
GND	1, <12:23>	I	Analog	0 V	Ground
VCC_I2C	30	I	Analog	+5 V	I^2C positive supply
GND_I2C	31	I	Analog	0 V	I^2C ground

Table 1.3: *Chipboard power supplies pinout*

1.3.2 Medipix2 physical description

The Medipix2 chip has been designed to minimize the dead area between chips covering large areas when butting several chips together. This is achieved by placing the periphery at the bottom of the chip (see Figure 1.6).

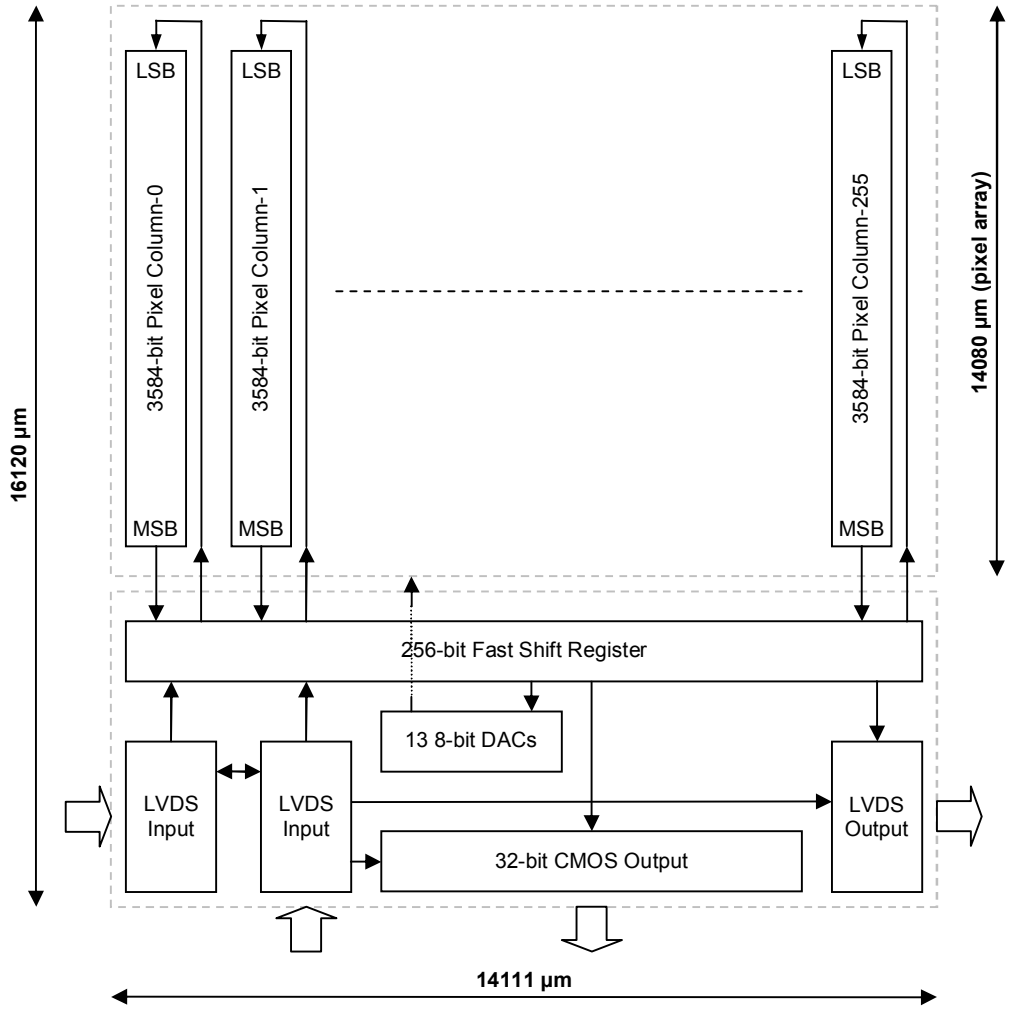


Figure 1.6: *Medipix2 surface plan and block diagram*

The non-sensitive area in the other three edges is minimized to less than 50 µm, so the various configurations of the butted chips can be made. The complete chip dimension is 16120 x 14111 μm^2. The sensitive area is composed of a matrix of 256 x 256 pixels of 55 x 55 μm^2 size each resulting in a detection area of 1.982 cm^2 which represents 87% of the entire chip area. At the bottom side of the chip there are 127 input/output pads. Most of them are wire bonded to the chipboard (see Table 1.2 and Table 1.3). The chip can be configured in serial mode and readout either serially or in parallel. However, the parallel read-out is not supported by current chipboard.

1.3.3 Medipix2 pixel cell

The Medipix2 cell occupies an area of 55 x 55 μm^2 and consists of 504 transistors. It can be divided into an analog and a digital part as shown in Figure 1.7. Both the analog and digital circuitry has been designed to operate with independent 2.2 V power supplies. The total power consumption is about 500 mW.

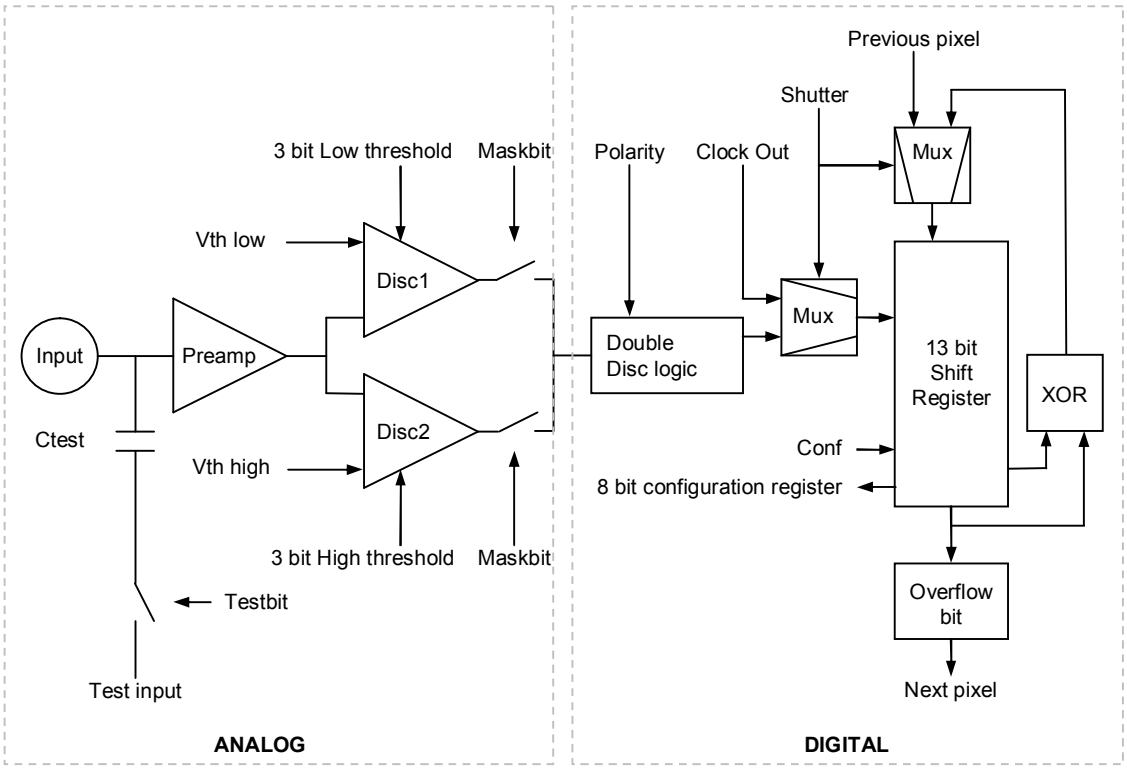


Figure 1.7: *Medipix2 pixel cell block diagram*

The analog part consists of a charge preamplifier with DC leakage current compensation, a test capacitance, and two branches of identical discriminators. The octagonal bump bond opening used for connection with sensor is placed on top of the analog side and has a diameter of 20 µm. The digital side contains the Double Discriminator Logic (DDL) and the 13-bit shift register with overflow bit. The pixel has two different working modes depending on the CMOS input *SHUTTER* state.

When the ***SHUTTER* signal is low** the pixel turns to data acquisition mode. In this case the shift register works as a pseudo-random counter of 13 bits with dynamic range of 8001 counts. The output of the double discrimination logic is used as clock for this

counter. When a charged particle interacts in the sensor depleted area it deposits a charge which drifts towards the collection electrode. This charge is then amplified and compared with two different thresholds. The comparators outputs are than connected to the DDL. This logic does the discrimination between two input signals and can work in two modes:

- **Single mode** is set when the high threshold level (Vth high) is set smaller than the low threshold (Vth low). In this case the output pulse is generated when a signal from the low discriminator is received. A high discriminator signal is in this case ignored.
- **Energy window mode** is set when Vth high is higher than Vth low. An output pulse is produced only when the signal from the low discriminator is obtained while the high discriminator remains quiet.

Every pulse coming from the discriminator logic increments the counter value by one unit. After the maximal value is reached (all bits are high again), the overflow bit is set to zero value. Each pixel can handle count rates of about 1 MHz. Read-out is performed after exposure to avoid dead time.

When the ***SHUTTER* signal is high** the pixel readout/setting mode can be initialized. In this mode the 14-bit shift register of each pixel is connected to the next and previous to form a 3584-bit shift register as shown in Figure 1.6. Communication between the pixel matrix and the IO logic is carried out through the 256-bit FSR[16]. For safety of this critical part, two independent and identical FSRs are implemented. Selection of a particular FSR is done by *SPARE_FSR*[17] input signal. When the *SHUTTER* is high an external clock can be used to shift the data from pixel to pixel. This mode is used both for setting the eight pixel configuration bits and for reading the 13-bit counter information.

1.3.4 Medipix2 IO operations

Medipix2 operation modes (see Table 1.4) are selected through *M0* and *M1* signals and are enabled by the falling edge of *ENABLE_IN* LVDS[18] signal. All control input must remain stable during every IO operation.

M0	M1	ENABLE_IN	SHUTTER	RESET	Operation
X	X	X	X	0	General reset of the chip
X	X	X	0	1	Counting
0	0	0	1	1	Reading-out the matrix
0	1	0	1	1	Setting the matrix
1	0	0	1	1	Setting the DACs
1	1	X	1	1	Resetting the matrix
0	1	X	0	1	Testing the Fast Shift Registers

Table 1.4: *Medipix2 IO operation modes*

[16] Fast Shift Register
[17] Description of the Medipix2 logic signals is given in Table 1.2
[18] Low Voltage Differential Signaling

1.3.4.1 General Reset

The low value of the CMOS input *RESET* induces the general reset of the Medipix2 chip. During the chip reset the LVDS drivers are not active, the FRS are set high, all IO counters are reset to the default values and all DACs are set to their mid-range value (default).

1.3.4.2 Counting mode

When the *RESET* signal is high and the *SHUTTER* signal goes low each pixel starts to count independently. Noisy pixels can be disabled through the mask bit in pixel configuration register. This pin is master for the rest of the control lines.

1.3.4.3 Serial read-out

The serial read-out mode is enabled by *ENABLE_IN* signal going low while *M0* and *M1* signals are low. Reading out operation is then performed by external clock through *FCLOCK_IN* LVDS input. The *P_S* pin controls the selection between parallel or serial readout mode and in the current type of chipboard must be always low.

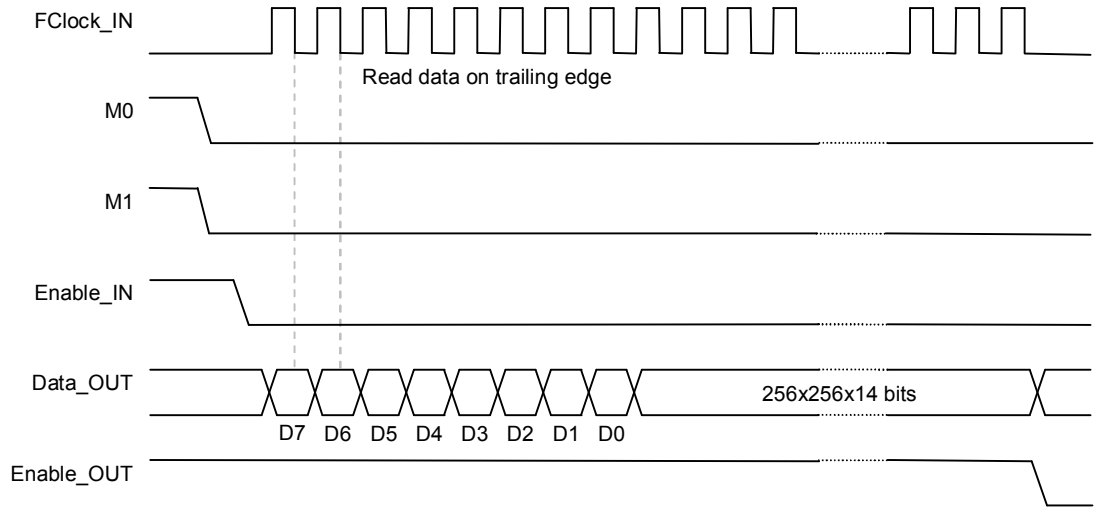


Figure 1.8: *One chip serial read-out diagram*

The serial readout uses a LVDS *DATA_OUT* port to shift out all the matrix data. To read the entire matrix, a total of 917512 (256 x 256 x 14 + 8) clocks are needed. The first eight bits must be sent due to the preload register. The rest of the clocks correspond to the number of bits in the entire matrix. Once the reading operation is finished the *ENABLE_OUT* signal is set to low value. The data on the output are valid on the falling edge of the *FCLOCK_IN* signal (see Figure 1.8).

The structure of acquired data is obvious from Figure 1.6. The eight preload register bits are followed by MSB[19] of the pixel from right-bottom corner (column 255)

[19] Most Significant Bit

followed by MSB of the neighboring pixel from column 254 and so forth. Last is LSB[20] of the pixel from left-upper corner of the chip.

1.3.4.4 Setting the matrix

Every pixel has the configuration register of eight bits size is used to set the parameters for each pixel cell independently. Six of these are used for fine threshold adjustment (three bits for each discriminator), one for masking noisy pixels, and one to enable the input charge test through the 8 fF on-pixel capacitance. The pixel configuration register structure in a 14-bit pixel shift register is shown in Figure 1.9.

Figure 1.9: *Configuration registers structure (MSB right)*

Setting *M0* low, *M1* high and *ENABLE_IN* going low the operation of setting of the configuration registers starts. The clock signal in *FCLOCK_IN* LVDS input performs the operation until the *ENABLE_OUT* falling edge signalizes the finish of writing the matrix. Once *ENABLE_IN* pin is set back high all the data in the pixel shift register is loaded in an 8-bit configuration register (static flip-flop). Unlike reading-out operation, in this case the input data is validated on leading edge of clock.

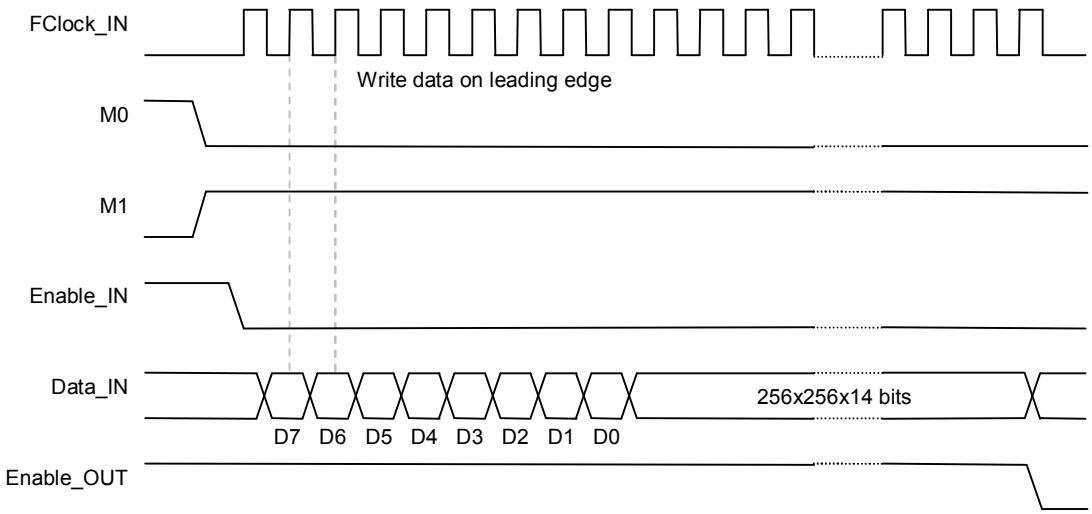


Figure 1.10: *One chip matrix setting diagram*

Due to preload register, eight dummy bits should be sent before the valid data. The number of clocks needed to set one chip is the same as for read-out operation.

1.3.4.5 Setting the DACs

This command is used to set the 13 on-chip integrated 8-bit DACs. This operation is initiated by *ENABLE_IN* going low while *M0* is set high and *M1* is set in low state.

[20] Least Significant Bit

The DACs values are set using the 256-bit FSR (Fast Shift Register). This register is loaded serially by the LVDS port (input data must be valid on leading edge of clock signal). After 8 + 256 clocks the *ENABLE_OUT* signal is set low and values from FSR are stored in an 8-bit parallel DAC registers. As we have 13 8-bit DACs, just 104 bits are needed to set in the 256-bit FSR. Table 1.5 shows the function and position of each DAC in the FSR.

DAC name	FSR position	DAC function
VbiasDelayN	$B3_{LSB}$-B10	Used to fix the pulse width at the counter input.
VbiasDisc	B11-B18	Sets the bias conditions in the discriminator amplifier.
VbiasPreamp	B19-B26	Sets the bias conditions in the preamplifier.
VbiasSetDisc	B45-B48, B55-B58	Sets the bias conditions in the fast discriminator logic.
VbiasThs	B59-B66	Sets the base current in the 3-bit threshold adjust circuitry.
VbiasIkrum	B99-B106	Sets the total DC current in the preamplifier feedback.
VbiasABuffer	B107-B114	Sets a common voltage for different analog buffers.
VthH	B115-B122	Sets the global high threshold voltage level.
VthL	B123-B130	Sets the global low threshold voltage level.
Vfbk	B131-B138	Sets the DC output preamplifier voltage.
Vgnd	B180-B187	Sets the DC voltage in the preamplifier positive input.
VbiasLVDStx	B226-B233	Sets the bias conditions for the LVDS output driver.
VrefLVDStx	B234-$B241_{MSB}$	Sets a voltage reference in the LVDS output driver.

Table 1.5: *Medipix2 internal DACs function and position in FSR*

Two special features can be done with the DACs, to sense out the value of each DAC and to use an external DAC to substitute any of the on-chip DACs. To perform one of these operations 5 bits from the FSR are used. Four DAC Code bits used for DAC identification are at positions $B37_{LSB}$, B38, B40 and $B41_{MSB}$ of the FSR. To bypass a selected internal DAC by an external one the B43 of the FSR is used. Setting this bit high substitutes a selected internal DAC by the *EXTDAC_IN* signal. The sense DAC function enables the connection of selected DAC to *DAC_OUT* pin which can be controlled by B42 of the FSR (active high). Because of the presence of a unity gain amplifier at the *DAC_OUT* pin, only voltage can be measured here. Table 1.6 shows the expected output voltage for each DAC.

Due to the differences between positive and negative charges collection some DACs have different values for this two collection modes. Vfbk node sets the DC output preamplifier voltage optimizing the dynamic range depending whether holes or electrons are being collected. A change in this voltage affects the overall gain of the preamplifier due to the change in the biasing point resulting in slightly different gains for the two collection modes. As the preamplifier output voltage is different, it is necessary to adapt the low and high threshold voltages (VthH and VthL) to fit the actual range. The polarity of collection is selected using the *POLARITY* input pad.

DAC name	DAC code	11111100	$10000000_{(DEFAULT)}$	00000011
VbiasDelayN	0001	290 mV	431.4 mV	461.5 mV
VbiasDisc	0010	535.2 mV	817 mV	925.7 mV
VbiasPreamp	0011	569.4 mV	983.1 mV	1.087 mV
VbiasSetDisc	0100	484.9 mV	728.5 mV	811.3 mV
VbiasThs	0101	1.711 V	1.425 mV	1.307 mV
VbiasIkrum	0111	1.761 V	1.537 V	1.462 V
VbiasIkrumHalf[21]	1000	368.8 mV	540.8 mV	579.2 mV
VbiasABuffer	1110	727.2 mV	900 mV	1.104 V
VthH	1100	Polarity low 607.2 mV Polarity high 1.274 V	Polarity low 721.8 mV Polarity high 1.425 V	Polarity low 855.5 mV Polarity high 1.594 V
VthL	1011	Polarity low 607.2 mV Polarity high 1.274 V	Polarity low 721.8 mV Polarity high 1.425 V	Polarity low 855.5 mV Polarity high 1.594 V
Vfbk	1010	Polarity low 417 mV Polarity high 1.365 V	Polarity low 600.2 mV Polarity high 1.605 V	Polarity low 836.9 mV Polarity high 1.909 V
Vgnd	1101	927.2 mV	1.099 V	1.302 V
VbiasLVDStx	0110	1.751 V	1.489 V	1.391 V
VrefLVDStx	1001	657.9 mV	1.040 V	1.694 V

Table 1.6: *External voltage DAC values*

1.3.4.6 Resetting the matrix

This operation sets all the counter bits high without affecting the pixel configuration registers. With *M0* and *M1* set high, 28680 cycle clocks (256 x 14 x 8 + 8) are needed to carry out this operation. Data input and output ports are inactive during this procedure, *ENABLE_OUT* pin low state signalizes the end of the operation.

1.3.4.7 Testing the FSR

This operation is used only for testing the functionality of the 256-bit Fast Shift Register. Having the same conditions than in the setting the matrix operation but with *SHUTTER* low, this operation just sends the data from the *DATA_IN* to the *DATA_OUT* LVDS ports through the FSR. If the received data is the same that the one sent out then the FSR is working properly. The one of the two on-chip FSRs can be selected by means of the *SPARE_FSR* pin. The functionality of FSR can be also tested by set matrix and then read matrix operations where the sent and received data should be identical.

1.3.4.8 Test pulse

This test structure is used to test the functionality of the pixel without an X-ray source and also to calibrate the entire active matrix. The test is active being *ENABLE_TPULSE* line high, and it is individually selectable for any pixel through the configuration register bit Test Bit (see Figure 1.9).

In each pixel there is included an 8 fF test capacitance (see Figure 1.7) to allow an individual input charge test using an external voltage pulse. Two external voltage inputs *ANIN_N02* and *ANIN_N04* are selectable through *ANIN_A1* signal.

[21] This DAC depends directly on VbiasIkrum DAC, but can be read individually

2 Hardware Design

This chapter describes the hardware development phase of the project. I will not give here the description of all the steps and circuits modifications that lead to the functional prototype but only the final solution is presented. Some problems solved during development are presented in chapter 4. The interface was designed to fulfill the following general requirements:

- Use USB bus for detector read-out and data acquisition control;
- PnP[1] and Hot-swap architecture;
- USB powered (including voltage source for detector bias);
- Serial read-out of Medipix2 chip (new chipboard support);
- Microprocessor controlled measurement;
- External triggering;
- Hardware timer;
- Temperature monitoring;
- Compact size of interface;
- Low cost.

2.1 Design strategy

The entire interface is controlled by a single chip microcontroller. To make a choice between lots of different available devices, additional requirements were imposed:

- High enough speed of the core to be able to feed the USB interface;
- Integrated USB controller;
- Integrated fast ADCs[2] to monitor the Medipix2 internal DACs and for back-side pulse sampling (see paragraph 4.2.2);

[1] Plug & Play
[2] Analog to Digital Converter

- Integrated DAC[3] for test pulse generation and Medipix2 DAC bypassing (higher than 8-bit precision would be an advantage);
- External interrupt input ;
- Two timers/counters for back-side pulse counting and triggering (see Figure 4.6) and for Medipix2 shutter timing;
- Integrated interfaces I^2C and SPI[4];
- Few external components;
- Compact dimensions;
- Low power consumption.

After market research with attention to the above mentioned requirements it was found, that there is no single chip microcontroller satisfying all of them. It is possible to use either microcontrollers with integrated USB 1.1 controller either with integrated ADC and DAC converters. As the variant with external analog converters would require more external components, the solution with external USB controller was selected. With consideration to component dimensions and cost the ADuC841 [12] microcontroller from Analog Devices was selected (for more detailed description see section 2.4).

There are various possible devices for realization of the USB interface. I chose the USB to parallel FIFO[5] bi-directional data transfer chip FT245BM [11] because it provides simple power control for the high power external devices powered via USB and the possibility of connecting an external EEPROM[6] for description strings storage (USB VID[7] and PID[8] numbers, serial number and the product description strings). The main advantage of this chip is that functional device drivers are provided royalty-free by manufacturer and the entire USB protocol is handled on-chip, so that no USB-specific firmware programming is required. The device is USB 1.1 and USB 2.0 compatible with data transfer rate 1 MByte/s.

2.2 Block diagram

On the base of above mentioned requirements the interface block diagram was created (see Figure 2.1). Communication between interface and control PC is realized via USB. USB also provides the power for supplying the interface and also the Medipix2 detector. The entire circuit can be divided into five main segments: USB interface with power control circuit, microcontroller with integrated ADC and DAC converters, electronics for logical levels conversion, high voltage source with current monitor circuit and other voltage sources (references).

[3] Digital to Analog Converter
[4] Serial Peripheral Interface
[5] First In First Out memory type
[6] Electrically Erasable Programmable Read Only Memory
[7] Vendor Identification
[8] Product identification

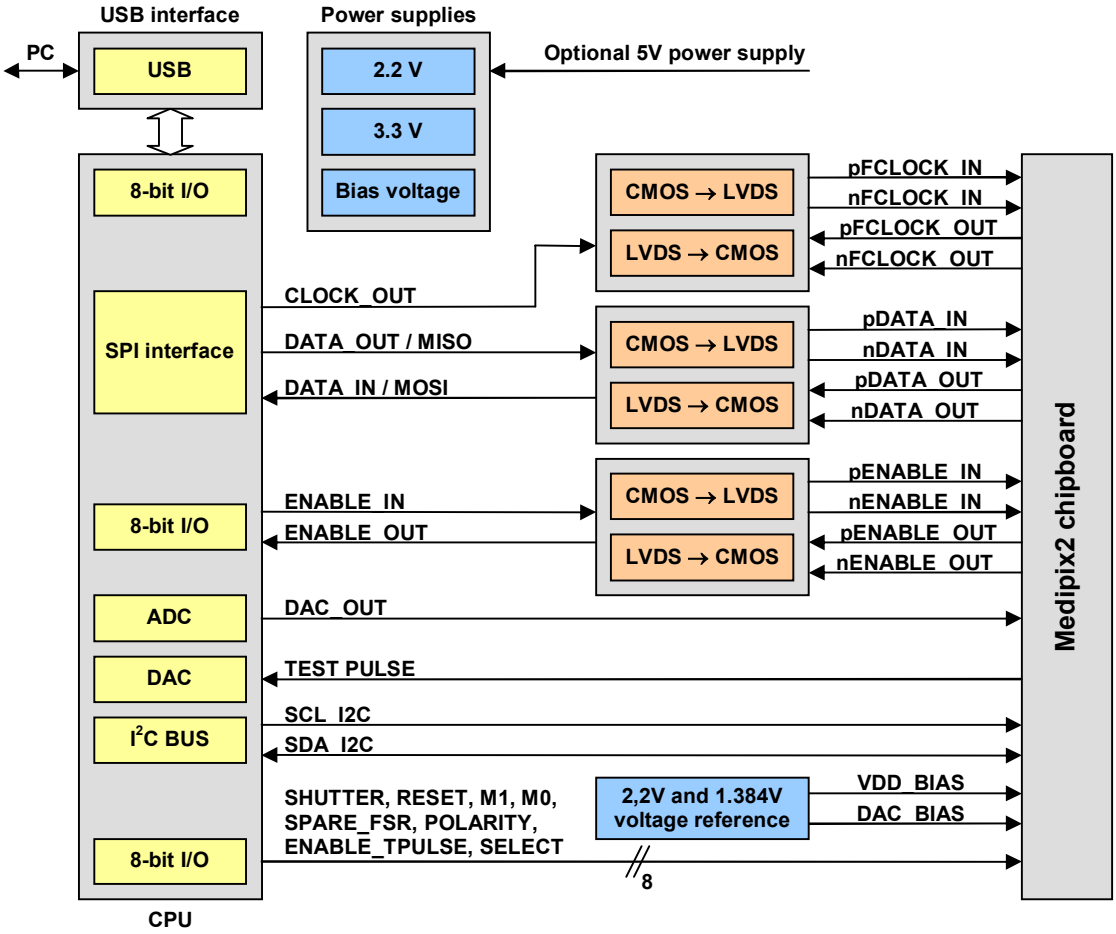


Figure 2.1: *USB interface block diagram*

2.3 USB interface

As was mentioned in subhead 2.1, the FT245BM [11] chip was selected to maintain the communication between the host PC and ADuC841 microcontroller. Every device connected via USB interface to the host PC must maintain the protocol specifications [22]. The protocol distinguishes between two basic types of devices. The self powered device has its own power supply and the USB cable is used only for communication whereas the bus powered device which takes the power directly from the USB host controller. Basic rules for bus power devices are as follows:

a) On plug-in, the device must draw no more than 100 mA.
b) On USB suspend mode the device must draw no more than 500 µA.
c) No device can draw more that 500 mA from the USB bus.

Figure 2.2 shows the wiring diagram of the USB interface with power control circuit for preserving the above mentioned rules.

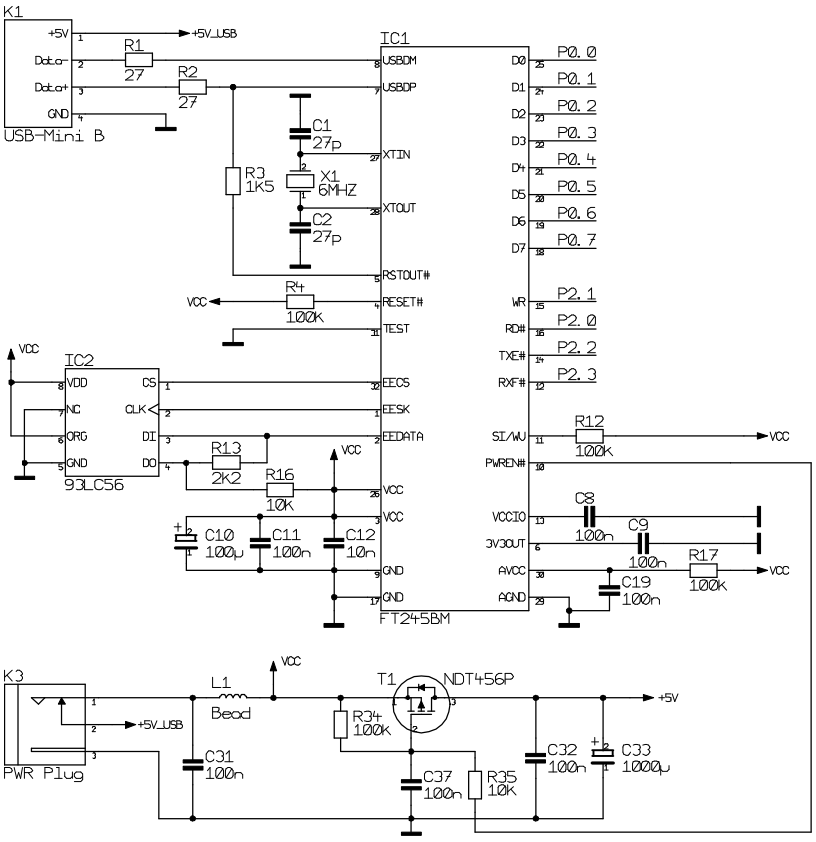


Figure 2.2: *USB interface with power control circuit*

After connecting of the USB cable the *PWREN#* pin goes high, so the P-channel MOSFET[9] transistor T1 is closed and the power to external logic circuits is turned off (so the current consumption is below 100 mA). When the device is configured via USB the *PWREN#* goes low. Resistor R35 and capacitor C37 prevents the current surge when the MOSFET turns on. Without this "soft start" circuit the power surge of the MOSFET turning on will reset the FT245BM, or the USB host hub controller. *PWREN#* pin also remains high during the USB suspend to keep the maximum current draw of 500 µA in this mode.

The Interface Pull-Down option in EEPROM must be enabled in this case to pull gently down the FIFO interface lines when the power is shut off (*PWREN#* is high). In this mode, any residual voltage on the external circuitry is bled to *GND* when power is removed thus ensuring that external circuitry controlled by *PWREN#* resets reliably when the power is restored.

Because the power consumption of the whole interface is higher than 100 mA the Maximum Power descriptor in the EEPROM must be set in to inform the host system of its power requirements (the value of 450 mA is used). The EEPROM programming utility MProg 2.3 [23] was used to configure all memory-based options.

For data transfer between the FT245BM chip and the microcontroller the port 0 is used. Four bits from port 2 are used to monitor the *TXE#* and *RXF#* status pins and generate the *RD#* and *WR* strobes.

[9] Metal Oxide Semiconductor Field Effect Transistor

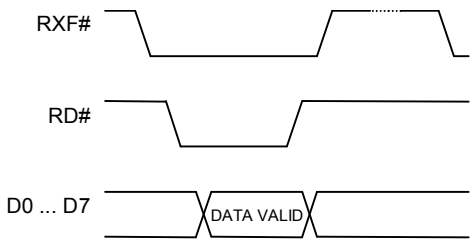


Figure 2.4: *FIFO read cycle*

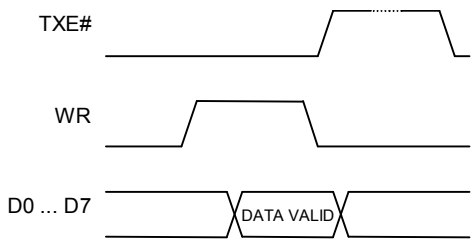


Figure 2.4: *FIFO write cycle*

When the host PC sends data to the microcontroller over USB, the data are stored in 128-byte receiving buffer and the device will take *RXF#* low to let the microcontroller know that at least one byte of data is available. Then the microcontroller can read a data byte at the leading edge of *RD#* pin (minimum pulse width is 50 ns). *RXF#* goes high after every byte read (see Figure 2.4).

To send data from the interface to the host computer, the microprocessor simply write the byte-wide data into the module when *TXE#* is low. Data must be valid at the trailing edge of *WR* pin. If the (384-byte) transmit buffer fills up or is busy storing the previously written byte, the FT245BM device keeps *TXE#* high in order to stop further data from being written until some of the FIFO data has been transferred over USB to the host PC. *TXE#* goes high when all data are written.

2.4 Microcontroller with ADC

The selected microcontroller ADuC841 [12] belongs to the 8052 family with backward compatibility with 8051 standard. Main features are following:

- **CPU core:**
  - Single-cycle 20 MIPS[10] 8052 based core;
  - 8051 compatible instruction set;
  - Up to 20 MHz external crystal;
  - 12 interrupt sources, 2 priority levels;
  - Three 16-bit timers/counters;
  - Dual data pointers, extended 11-bit stack pointer;
- **Memory:**
  - Up to 62 kBytes on-chip Flash/EE program memory;
  - 4 kBytes on-chip Flash/EE data memory;
  - 2304 bytes on-chip data RAM;
- **Analog I/O:**
  - 8-channel, 420 kSPS high accuracy, 12-bit ADC;
  - On-chip, 15 ppm/°C voltage reference;
  - DMA controller, high speed ADC-to-RAM capture;
  - Two 12-bit voltage output DACs;
  - Dual output PWM ∑-Δ DACs;
  - On-chip temperature monitor function;

[10] Million Instructions Per Second

- **Digital I/O:**
  - Four 8-bit I/O ports (multiplexed with alternate functions);
- **On-chip peripherals:**
  - Time interval counter (TIC);
  - UART[11], I^2C and SPI Serial I/O;
  - Watchdog timer (WDT);
  - Power supply monitor (PSM);
- **Power consumption (core CLK = 20 MHz):**
  - Normal mode: 45 mA @ 5 V;
  - Idle mode: 12 mA @ 5 V;
  - Power-down mode: 50 μA @ 5 V;
- **Package:**
  - 8 mm × 8 mm chip scale package;
  - 52-Lead Plastic Quad Flat Package [PQFP];
  - 56-Lead Frame Chip Scale Package [LFCSP].

Pins of the microcontroller can be divided into digital and analog ones. Usage of each pin of the **digital part of the microcontroller** is described in the following table:

ADuC841[12]		**I/O**	**Signal**	**Description**
Name	**Num**			
P0.0/AD0	46	I/O	D0 / RESET	Port 0 of the microcontroller is used for data transferring from/to FT245BM and also for Medipix2 CMOS inputs driving (through the latch IC6).
P0.1/AD1	47	I/O	D1 / ANIN_A1	
P0.2/AD2	48	I/O	D2 / ENABLE_PULSE	
P0.3/AD3	49	I/O	D3 / POLARITY	
P0.4/AD4	52	I/O	D4 / SPARE_FSR	
P0.5/AD5	53	I/O	D5 / M1	
P0.6/AD6	54	I/O	D6 / M0	
P0.7/AD7	55	I/O	D7 / SHUTTER	
P2.0/A8/A16	30	O	RD#	FT245BM read pulse input
P2.1/A9/A17	31	O	WR	FT245BM write pulse input
P2.2/A10/A18	32	I	TXE#	Can write to FT245BM if low
P2.3/A11/A19	33	I	RXF#	Can read from FT245BM if low
P2.4/A12/A20	39	O	LE	Latch enable/disable (IC6)
P2.5/A13/A21	40	I	ENABLE_OUT	Medipix2 LVDS output
P2.6/PWM0/A14/A22	41	O	ENABLE_IN	Medipix2 LVDS input
P2.7/PWM1/A15/A23	42	O	P2.7	Power enable inputs (IC12, IC13)
P3.0/TXD	18	I/O	P3.0/TXD	General purpose / UART
P3.1/RXD	19	I/O	P3.1/RXD	General purpose / UART
P3.2/INT0#	20	I/O	P3.2/INT0#	General purpose / External trigger
P3.3/INT1#/MISO	21	I	DATA_OUT	Medipix2 LVDS output
P3.4/T0/PWMC	24	I/O	SDA_I2C	I^2C bus data line
P3.5/T1/CONVST#	25	I/O	P3.5/T1	General purpose / Timer input
P3.6/WR#	26	O	SCL_I2C	I^2C bus clock signal
P3.7/RD#	27	O	CS#	SPI enable input of IC15
SCLOCK	28	O	FCLK_IN	Medipix2 LVDS input
SDATA/MOSI	29	O	DATA_IN	Medipix2 LVDS input

Table 2.1: *Digital signals connection of ADuC841 microcontroller*

[11] Universal Asynchronous Receiver/Transmitter
[12] Pin numbers is corresponding to 56-Lead Frame Chip Scale Package [LFCSP]

Port 0 of the microcontroller is used in two ways. The first way is used for communication between MCU[13] and FT245BM chip (when it is allowed by *TXE#* or *RXF#* signals). During the communication the *LE* signal driven by P2.4 pin must stay low. In the second mode when the *LE* pin is high the 74LCX573 is enabled (see following chapter 2.5) and can be used to the change setting of CMOS inputs of the Medipix2 device. In this case, the *RD#* and *WR* signals must be quiet.

Also the SPI interface is utilized for two purposes. The first, it is used for serial communication with the Medipix2 device. The second, for high voltage (HV) settings (see chapter 2.6). In case of the Medipix2 serial communication the *CS#* signal controlled by P3.7 pin must be set high. When the high voltage setting is required, the *CS#* signal goes low to enable the SPI inputs of MAX1932. The *ENABLE_IN* signal, which starts the Medipix2 serial data transmission, must stay high until the data transfer to the HV source is finished.

The wiring diagram of the **analog part of the microcontroller** is shown in Figure 2.5. The analog part of the microcontroller and also other analog circuitry (operational amplifiers) is powered from the *AVDD_uP* supply line to prevent the noise from digital part of the MCU.

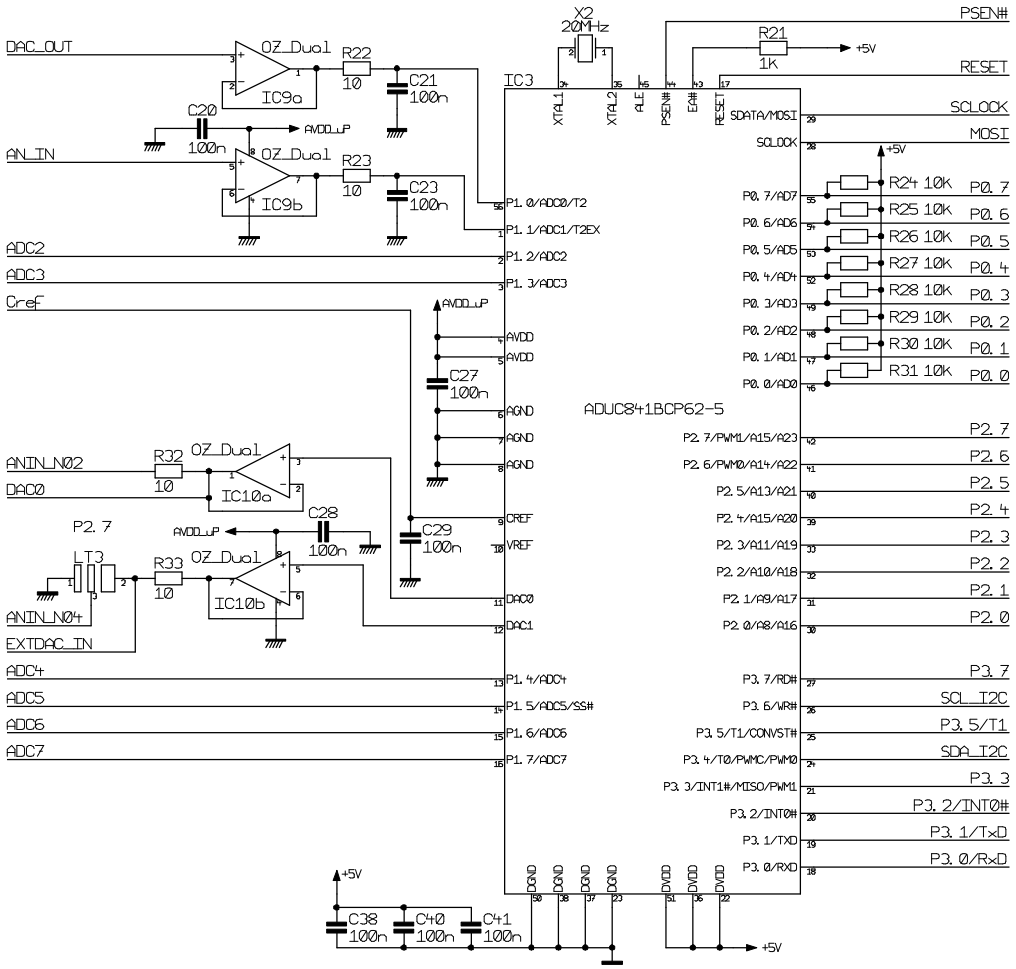


Figure 2.5: *Analog part of the microcontroller*

[13] MicroController Unit

Connection of the single analog pins is described in the following Table 2.2. The first two ADC inputs are connected through the voltage follower and additional RC couple. Though the RC does help to reject some incoming high frequency noise, its primary function is to provide a capacitive bank from which the integrated 32 pF sampling capacitor can draw its charge. This solution permits the fastest conversion speeds[14]. Input of the second voltage follower *AN_IN* and also the last four ADCs are directly linked to the internal analog connector for future upgrade purposes.

The DAC outputs are buffered to enable the possibility of driving more significant loads. First DAC is used for generating the test pulse signal *ANIN_N02* for Medipix2 purposes. The second test pulse analog input *ANIN_N04* can be through LT3 solder pads connected either to the DAC1 output or to the analog ground enabling the DAC1 to be used for bypass one of the Medipix2 internal DACs.

ADuC841[15]		**I/O**	**Signal**	**Description**
Name	**Num**			
P1.0/ADC0/T2	56	I	DAC_OUT	Medipix2 internal DACs measurement
P1.1/ADC1/T2EX	1	I	AN_IN	Internal analog connector (buffered input)
P1.2/ADC2	2	I	ADC2	High voltage output measurement
P1.3/ADC3	3	I	ADC3	High voltage current sense
P1.4/ADC4	13	I	ADC4	Internal analog connector
P1.5/ADC5/SS#	14	I	ADC5	Internal analog connector
P1.6/ADC6	15	I	ADC6	Internal analog connector
P1.7/ADC7	16	I	ADC7	Internal analog connector
DAC0	11	O	ANIN_N02 / DAC0	Test pulse input 1 / Internal analog connector
DAC1	12	O	ANIN_N04 / EXTDAC_IN	Test pulse input 1 / Medipix2 internal DAC bypass

Table 2.2: *Analog signals connection of ADuC841 microcontroller*

2.5 Logical levels conversion

Previous two subheads describe the communication between control PC and MCU. These devices can be connected easily, because both use the TTL[16] 5 V logic levels, so no additional voltage levels converters are needed in this case. Different situation is between microcontroller and Medipix2 device where some logical levels conversion electronics must be used (see Figure 2.6).

[14] For further information see [12], p.27
[15] Pin numbers is corresponding to 56-Lead Frame Chip Scale Package [LFCSP]
[16] Transistor Transistor Logic

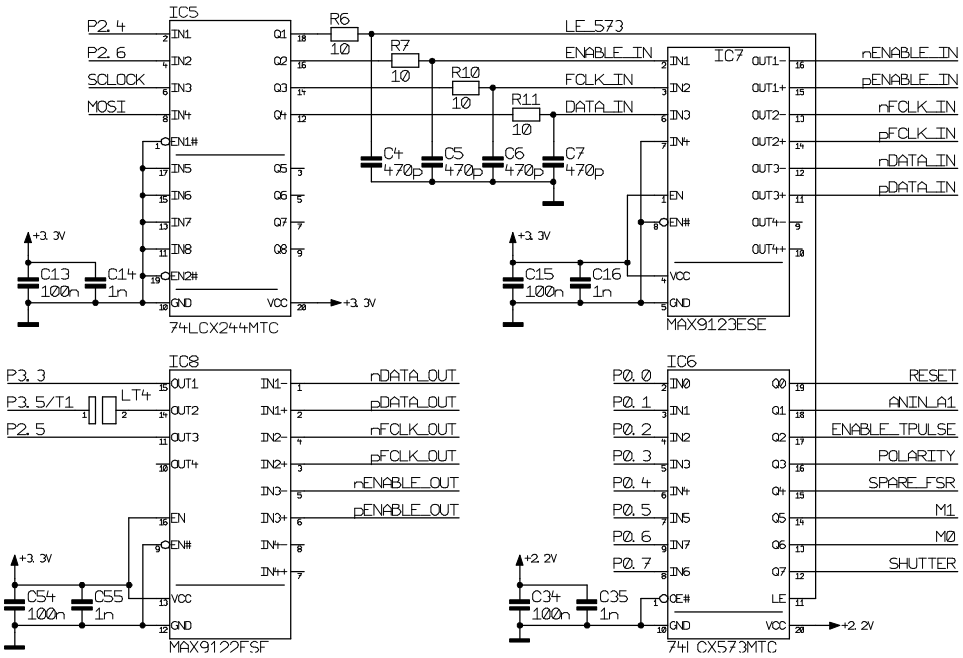


Figure 2.6: *Logical levels conversion electronics*

First of all it is necessary to convert LVSD[17] signals to CMOS to enable serial communication. MAX9122 quad LVDS line receiver with integrated termination [12] and MAX9123 quad LVDS line driver [14] was chosen for this purpose. Flow-through pinout of both circuits simplifies the printed circuit board layout and reduces crosstalk by separating the LVDS and LVTTL[18] signals.

Unfortunately, LVDS drivers and receivers use low voltage logic which defines maximum input voltage to 3.3 V (see Table 2.3). Due to this limitation the MCU output voltage must be decreased properly. Various possible solutions were tested (from a resistor divider to transistor switch) but the best solution was to use a buffer or line driver from one of the low voltage families [18], which has the capability to interface with 5 V logic on the inputs, outputs, or both. The 74LCX244 [15] device containing eight non-inverting buffers with 3-state outputs was selected. The rectifying RC filters (R6 + C4 etc.) are connected to the buffer outputs because the current surge during switching off the circuit causes the output voltage instabilities which produce the communication problems. Table 2.3 clarifies that the inverse signal direction (from LVDS receiver to MCU) is connectable directly.

Device	Input				Output			
	L_{MIN}	L_{MAX}	H_{MIN}	H_{MAX}	L_{MIN}	L_{MAX}	H_{MIN}	H_{MAX}
FT245BM	0 V	1 V	2 V	5 V	0 V	0.7 V	4.4 V	5 V
Microcontroller	0 V	0.8 V	2 V	5 V	0 V	0.4 V	2.4 V	5 V
LVDS	0 V	0.8 V	2 V	3.3 V	0 V	0.3 V	2.7 V	3.3 V
Medipix2	0 V	0.7 V	1.5 V	2.2 V	-	-	-	-

Table 2.3: *I/O logical voltage levels*

[17] Low Voltage Differential Signaling
[18] Low Voltage Transistor Transistor Logic

The same problem is in case of connection between the MCU outputs and the Medipix2 CMOS inputs which select the Medipix2 operation modes (see chapter 1.3.4). Because during the serial communication between detector and microcontroller these signals have to remain stable a low voltage octal latch with 5 V tolerant inputs and outputs 74LCX573 [16] was selected. The voltage power supply for the latch is 2.2 V to ensure that the Medipix2 high input voltage will be proper.

2.6 High voltage source and current monitor

An important feature of the new interface is the integrated high voltage source for the detector bias. It is based on the MAX1932 chip [18], which is originally designed for a power supply to bias avalanche photodiodes in optical receivers. The chip perfectly matches our requirements. MAX1932 uses a constant frequency of 300 kHz, pulse width modulated (PWM) boost architecture for generation low ripple output voltage from 5 to 90 V. The 8-bit SPI[19] compatible internal DAC allows controlling output voltage digitally in 255 steps (value 00h is used to shut down the converter). Figure 2.7 shows the wiring diagram of the bias source.

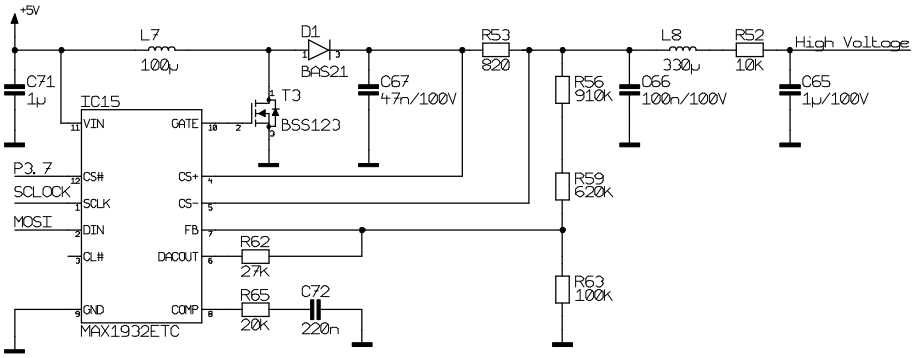


Figure 2.7: *High voltage source circuit*

The components values are calculated for 5 V input voltage, the output voltage spans from 20 V to 90 V with 2 mA output current. The output current is monitored at a sense resistor R53 by *CS+* and *CS-* pins. When the voltage drop at R53 exceeds 2 V (a typical value) it causes the output voltage limitation. The output voltage is given by feedback resistor divider coupled through R62 with DACOUT signal. Minimum output voltage V_{OUT_FFh} is selected by setting the DAC registers to FFh value, value 01h corresponds to the maximum output voltage V_{OUT_01h}. Resistor (R56 + R59) sets the adjustment span of the output voltage using the following equation:

$$(R56 + R59) = (V_{OUT\_01h} - V_{OUT\_FFh}).(R62/1.25)$$

The minimum output voltage is set by R63 value with this equation:

$$R63 = ((1.25 \times (R56 + R59))/V_{OUT\_FFh}$$

[19] Serial Peripheral Interface

The sense resistor R65 is, with capacitor C65, used as a part of output lowpass filter. An additional filter composed from L8, R52 and C65 is added for a further reduction of output noise and ripple.

As it was said above, the SPI interface of the microprocessor is used for the output voltage setting. Because the same signals are utilized for the Medipix2 serial communication, the *CS#* pin of MAX1932 must be used to control a selection of the target device. The low state of the control pin enables the MAX1932 communication while the Medipix2 is quiet. Figure 2.8 shows the timing diagram of the communication. In this case the data must be valid on the leading edge of clock signal.

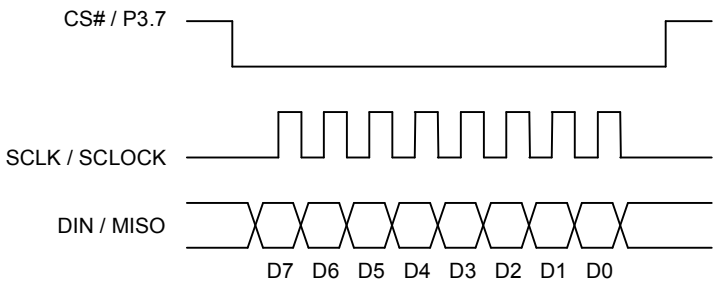


Figure 2.8: *MAX1932 serial interface timing diagram*

The voltage measurement and the current monitoring circuits are situated next to the high voltage filtering circuit (see Figure 2.9). Two resistor dividers form the measuring bridge[20] for monitoring the high voltage output current. The trimmer TR2 is assigned for the bridge balancing. The differential amplifier IC16b with the voltage gain about 10 times is used to sense the voltage drop at R51. The second operational amplifier IC16a is connected as a voltage follower to measure the output high voltage. Outputs of the operational amplifiers are connected to the microcontroller's integrated ADC. The resistor dividers are selected so that the operational amplifiers output voltage can be up to 2.5 V at maximum.

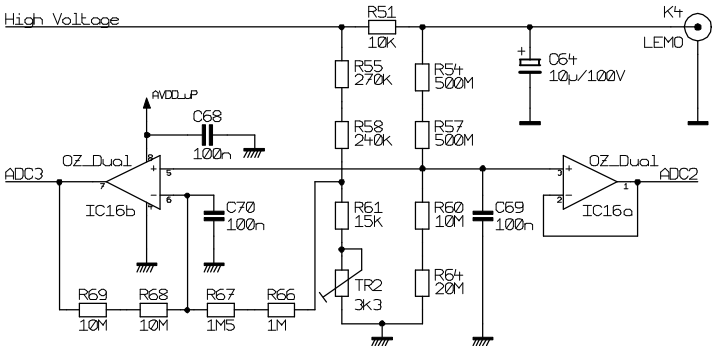


Figure 2.9: *High voltage and current monitor circuit*

[20] There are two serially connected resistors in each bridge arm so that the bridge can be balanced more easily.

2.7 Power supplies and voltage reference

This is the most critical part of the interface, because the Medipix2 detector is very sensitive to any voltage instabilities during the measurement or serial communication.

The first of all there is a restriction for USB cable for connection to a host PC. Since all the power needed for the interface and the Medipix2 detector is conducted via the USB cable and the minimal operating voltage for microcontroller is 4.75 V the cable with resistance less then 0.5 Ω must be used. This value can be reached by reducing the cable length or increasing the diameter of the power wires. There are also differences between the USB host controllers (output voltage is not always exactly 5 V), so in this case the self powered USB hub or external power source must be used to ensure the interface functionality.

Because the interface is intended to be used with portable devices, which are in many cases battery powered, the design of the power sources allows turning off the power to Medipix2 detector and all the related electronics except microcontroller and FT245BM chip to reduce the power consumption. This feature is controlled by MCU through the P2.7 pin. For the same reason and also to reduce the heat dissipation of the interface the DC-DC step-down converter MAX1951 [17] is used before linear regulator for Medipix2 2.2 V power supply. In case of problems with the DC-DC converter it does not have to be mounted and only linear regulation can be used. To fulfill all these requirements the circuit shown at Figure 2.10 was designed.

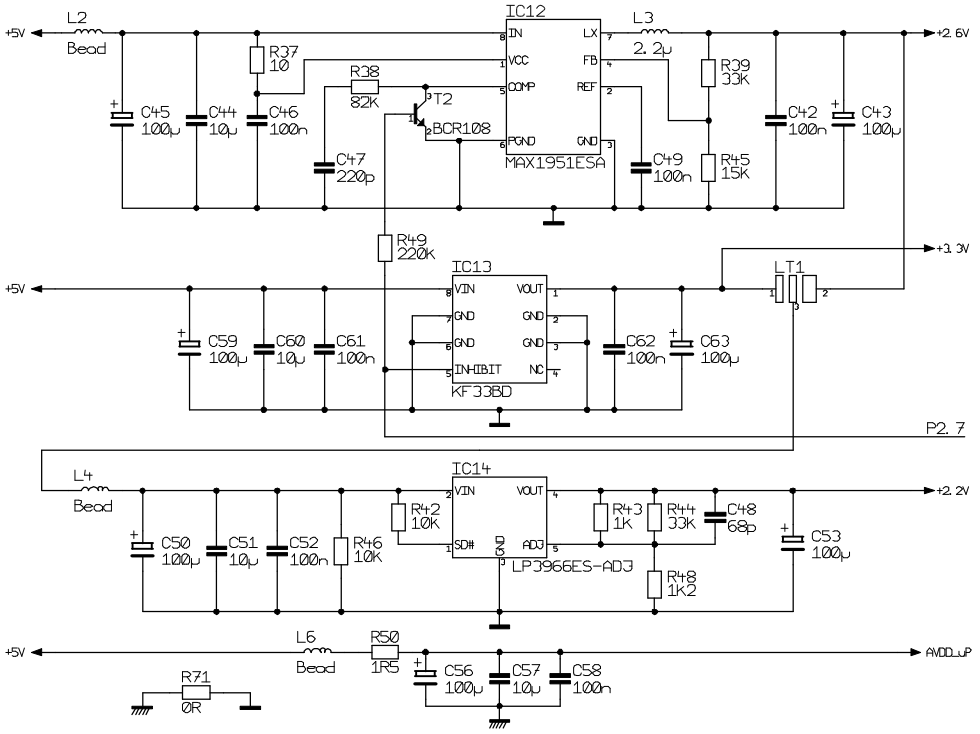


Figure 2.10: *Power supplies*

Therefore three different voltage sources for Medipix2 detector and related electronics are needed:

- 5 V is obtained directly from the USB interface for the microcontroller, operational amplifiers and FT245BM device power supply. The analog part of the MCU and all operational amplifiers are powered through a lowpass filter consisting of the ferrite bead L6, the serial resistor R50 and capacitors C56 to C58.
- 3.3 V is provided by the linear voltage regulator KF33BD (maximal output current is 500 mA). This voltage is used for supplying the LVDS driver MAX9123, LVDS receiver MAX9122 and the octal buffer 74LCX244.
- 2.2 V for Medipix2 digital and analog (additional filter is used) power supplies. The input 5 V voltage from the USB bus is primarily reduced by DC-DC converter MAX1951 to the value of approximately 2.6 V. Then the fast adjustable ultra low dropout linear regulator LP3966ES-ADJ (IC14) is used to obtain the appropriate voltage for Medipix2 detector. In case of instability of the DC-DC converter the input of IC14 can be connected to the 3.3 V output of the linear regulator KF33BD.

Like for any other regulator external capacitors are required to assure stability. These capacitors must be correctly selected to reach the proper performance. The equivalent serial resistance (ESR) of the input capacitors for all three voltage sources has to be as small as possible, so the parallel combination of low ESR polymer tantalum capacitors (45 mΩ at 100 kHz) and ceramic capacitors is used. The low ESR of the output capacitor in DC-DC circuit is also desirable, so the same combination is used. In case of linear regulators, the ESR of the output capacitors cannot be so low because it forms a zero to provide phase lead which is required for loop stability. In this case the tantalum electrolytic capacitor with ESR value of 0.4 Ω is used. All the capacitors are selected to meet the requirements for minimum amount of capacitance and also an appropriate ESR value over the full tolerance and temperature range of the application.

The analog and digital power supplies of the microcontroller (*AVDD_uP* and *+5 V*, respectively) are separated by a small series resistor and ferrite bead (see the bottom of the Figure 2.10) to allow the analog supply line to be kept relatively free of the noisy digital signals that are often present on the system digital power supply line. This configuration ensures that the difference between *AVDD_uP* and *+5 V* lines remains within ±0.3 V of one another at all times to avoid damaging the chip.

Additional voltage references for the Medipix2 purposes are needed. Firstly, the bias reference voltage for on chip DAC of value 1.384 V is needed at *DAC_BIAS* pin. The additional 2.2 V voltage reference is used for the *DAC_BIAS* mirroring. The micropower 3-terminal adjustable band-gap voltage reference diode LM385 was chosen (see the wiring diagram in Figure 2.11). It is operating from 1.24 V to 5.3 V and over a 10 μA to 20 mA current range. Since the LM385 band-gap reference uses only transistors and resistors low noise and good long-term stability were reached.

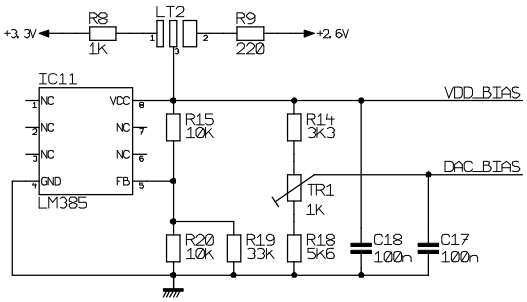


Figure 2.11: *Voltage reference*

As the Medipix2 chip demands the stabile voltage reference between *VDD_BIAS* and *DAC_BIAS* signals, only one the LM385 circuit is used[21] to obtain the 2.2 V for *VDD_BIAS* and then the resistor divider decreases this voltage to value of 1.384 V for the *DAC_BIAS*.

In the normal operation mode the voltage reference is connected to the DC-DC converters output. In case of a interference from DC-DC converter there is a possibility to connect the voltage reference via LT2 solder pads to the output of the linear 3.3 V regulator IC14.

2.8 I/O connections of the interface

All the abovementioned components are mounted on four layers PCB[22] (see interface layout diagram at Figure 2.12). The wire diagram of the whole interface is presented in appendix A.3.

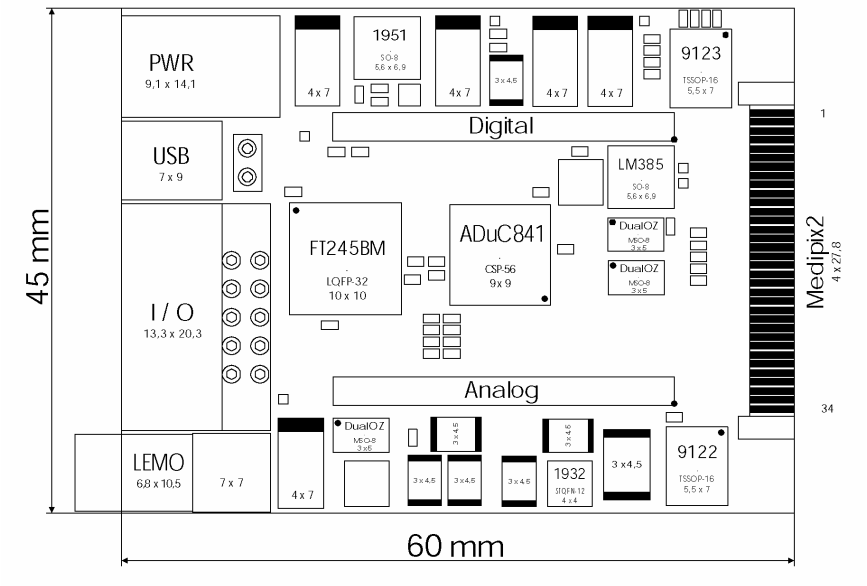


Figure 2.12: *Diagram of the interface layout*

[21] There are two LM385 circuits used for the same purpose at the MUROS2 interface
[22] Printed Circuit board

Because the counterpart to the 68-pin VHDCI[23] connector used on Medipix2 chipboard is not available in the PCB version (only in the cable version), the connection pads are created on the right side of the PCB. Leading groove is milled out in the interface board next to connection pads, so the Medipix2 chipboard can be plugged directly to the interface board. On the left side of the interface PCB are situated all the external interface connectors:

- PWR connector for optional 5 V power supply;
- USB Mini-B connector for power supplying and communication between interface and the host PC;
- LEMO connector (type EPL.00.250.NTN) for detector bias high voltage output;
- I/O – 10-pin standard computer connector to PCB with 5-pins in two rows for software loading, debugging and external triggering. Also UART and I^2C signals are connected here.

There are also two internal connectors (analog and digital one mounted next to the microcontroller). These connectors can be used to attach of additional plug-in modules to extend the interface functionality. This solution can be with benefit used for connection of separately shielded charge sensitive preamplifier enabling back side pulse spectroscopy (see Figure 4.6). Also other modules can be attached for other application requirements (additional memory module, stepper motors control, etc.).

On the left side of the PCB a LED diode signalizes communication via the USB bus. The whole interface is placed in a duralumin box with dimensions of 50 x 80 x 20 mm.

[23] Very High Density Cable Interconnect

3 Software Development

The software development phase of the project, described in this chapter, can be divided into the microcontroller and control PC part. I was responsible for development and debugging of the assembler based software for the microcontroller. Software for communication with the control PC is described at the end of the chapter.

3.1 In-circuit serial download access

One of the many ADuC841 microcontroller features is an ability to download code to its on-chip FLASH/EE program memory while being still 'in-circuit'. This in-circuit code download feature is conducted over the device UART serial port and is thus commonly referred to as 'serial download'. Serial download capability allows reprogramming of the part while it is soldered directly onto the target system avoiding the need for an external device programmer and the requirement for having to remove the device to use the external programmer. Serial download also opens a possibility to upgrade the system firmware in the field without having to swap out the device.

Also built into the part is a dedicated controller for single-pin in-circuit emulation. In this mode the emulation access is gained by connection to a single pin (*EA* pin is used) to ensure that all the resources of the microcontroller are available for programming. This possibility was not used because a special external emulator circuit is required to enable this feature.

The microcontroller can be configured for serial download mode via a specific pin configuration at power-on or application of the external reset signal. If the *PSEN* input pin of the microcontroller is pulled low through a resistor (1 kΩ) on power-on or during application of a hard reset input then the microcontroller will enter serial download mode[1]. In this mode an on-chip resident loader routine is initiated, the on-chip loader configures the device UART appropriately and, via a specific serial download protocol

[1] For enabling the possibility of entering the serial download mode the PSEN and RESET pins are connected to the external I/O connector

[18] will communicate with any host machine to manage the download of data into its FLASH/EE memory spaces. The serial download mode operates within the nominal supply rating of the part and as such there is no requirement for a specific external high programming voltage, as this is also generated on-chip. Connecting a PC to the microcontroller chip for downloading or debugging code requires an RS-232 line driver/receiver chip to step CMOS logic levels of the integrated UART up to RS-232 levels [21].

3.2 Development tools

The QuickStart development kit from Analog Devices was used for the design of the prototype interface. The development system consists of the following PC based (Windows compatible) hardware and software development tools:

Hardware

- Evaluation Board
- Serial Download/Debug Cable
- International Power Supply

Software

- Metalink 8051 Cross Assembler
- Accutron "Aspire" IDE[2] Featuring Assembly-Source Debugging and Simulation
- Serial Downloader
- Analog Performance Analysis Package
- Example Code, Function Libraries, Datasheets, Application Notes, Etc.

3.2.1 Metalink 8051 cross assembler

The Metalink 8051 Cross Assembler serves for the compilation of the assembly language source code created with a text editor. It takes an assembly language source file, saved with a .ASM extension and creates two files, an output list file (.LST) and a machine language object file in standard Intel hexadecimal format (.HEX).

The list file output (.LST) displays the results of the assembler operation, including any syntax or other errors present in the original source code.

The Intel Hex file (.HEX) is used to program the part using the Windows Serial Downloader (WSD) as described in section 3.2.3.

3.2.2 Aspire IDE

The Accutron Aspire Integrated Development Environment is a Windows application that allows the user to compile, edit, and debug code in the same environment using the microcontroller UART serial port. The debugger provides access to all on-chip peripherals during a typical debug session as well as single step, animate, and break-point code execution control.

[2] Integrated Development Environment

The Aspire environment is capable of full C-source debug and non-intrusive single pin emulation, but the version included in the QuickStart development kit supports assembly level serial debug only.

3.2.3 Windows serial downloader

The Windows Serial Downloader (WSD) is a Windows application that allows the user to serially download an assembled program (Intel hexadecimal format file) to the on-chip FLASH/EE program memory via the serial port (COM1 to COM4) on a standard PC. It should however be emphasized that any master host machine (PC, other microcontroller, DSP or other) can download to the ADuC841 microcontroller once the host machine adheres to the specified serial download protocols (for detailed information see the application note [18]). The WSD also incorporates the protocols for downloading to FLASH/EE data memory, setting of security bits and various RUN options.

3.2.4 Windows analog software program

The Windows Analog Software Program (WASP) is a general application for all ADuC family products that allows analysis of their analog performance. The WASP recognizes which type of microcontroller the PC is communicating with, before automatically downloading the appropriate code. After downloading the code the WASP launches the acquisition window. This allows the user to configure, control and analyze the ADC noise performance with the various analog and digital peripherals enabled/disabled.

3.3 Software structure

As it was mentioned above, the source code for the microcontroller control software was written in assembler. Because of significant extent of the program (size of source code in assembler is about 50 kB) I will not describe functionality of the whole software here. Only the software command structure and some example command service is described in following subheads.

3.3.1 Command service organization

After the power-on or hard reset of the ADuC841 microcontroller the initialization procedure was started. In this procedure all interrupt sources are disabled and the state of special registers of the microcontroller is set appropriately. By force of this special function registers the properties of microcontroller peripherals are set (e.g. interrupt sources enabling and priorities, ADC and DAC settings, UART and SPI configuration, etc.). This initialization procedure is followed by the main endless loop (see Figure 3.1).

```
;-------------------------------------------------------------------------------
; Main Endless loop - waits for command character received via USB

WaitForCommand:
    CALL  FT_GetChar      ; Wait for any character to be received by FTDI
    MOV   B,A             ; Store received command to B register
    MOV   DPTR,#Com_Table ; DPTR points to command table

  TestItem:
    CLR   A               ; Clear accumulator
    MOVC  A,@A+DPTR       ; Read a command from the table
    INC   DPTR            ; Set DPTR to point to command service routine address
    JZ    UnknownCom      ; End of table => go to UnknownCom
    CJNE  A,B,NextItem    ; This is not just received command => go to NextItem

    ; This is the command => after command code there is address of the command service
    CLR   A               ; Clear accumulator
    MOVC  A,@A+DPTR       ; Read lower half of command service address
    MOV   R1,A
    INC   DPTR            ; Increment DPTR
    CLR   A               ; Clear accumulator
    MOVC  A,@A+DPTR       ; Read higher half of command service address
    MOV   R0,A            ; Registers R1 and R0 contains address of the command service

    MOV   DPTR,#WaitForCommand
    PUSH  DPL
    PUSH  DPH             ; Address of the WaitForCommand is stored in the stack (return
                            address from command service routine)
    PUSH  00
    PUSH  01              ; Address of the command service routine is in the stack
    RET                   ; Jump to service, service has to end with RET instruction to
                          ; jump to WaitForCommand

  NextItem:
    INC   DPTR            ; Skip the first part of the command service routine address
    INC   DPTR            ; Skip the second part of the command service routine address
    JMP   TestItem        ; Check next table item

  UnknownCom:
    MOV   DPTR,#STR_UnknownCom
    CALL  FT_SendString   ; Send the unknown command message via USB
    JMP   WaitForCommand  ; Jump to the begin of the loop
;-------------------------------------------------------------------------------
```

Figure 3.1: *Main endless loop – waiting for command character receiving*

In the main endless loop the microcontroller is waiting for a command character to be received via the USB. When the character is obtained, it is compared with the table of known characters (see table structure in Figure 3.2). Every item in the table consists of three bytes. The first byte is an ASCII[3] code of the command character the second and third byte forms the command service subroutine address. The last command has to be 00h indicating end of the table.

```
;-------------------------------------------------------------------------------
Com_Table:
    DB 'r'
    DW ComServ_Reset
    .
    .
    DB 'b'
    DW ComServ_SetBias
    DB 0
;-------------------------------------------------------------------------------
```

Figure 3.2: *Command table*

[3] American Standard Code for Information Interchange

When the **received command is found** in the table the address of its service subroutine is copied to the registers R1 and R0. Then the address of the main endless loop entry point is stored on the top of the stack. The command service address is pushed to the stack as well and the RET instruction is executed. During the RET command the address at the top of the stack is fetched and program jumps to the command service subroutine. The service of each command has to be terminated by another RET instruction which ensures that the program execution returns to the main endless loop.

When the **received command is not found** in the table, than the 00h command at the end of the table cause sending of the appropriate error message to the host PC and program returns to the main endless loop.

The following Table 1.1 shows the list of basic commands and their descriptions. Note, that the software is not at final state, so that new commands can be easily added if required.

Command label	Character	Command description
Reset	r	Reset the Medipix2 device
SetMatrix	s	Set the Medipix2 configuration matrix
EraseMatrix	e	Erase the matrix
ReadMatrix	m	Read the matrix
SetDACs	d	Set the integrated DACs of the Medipix2 detector
TestFSR	f	Test the fast shift register
OpenShutter	o	Open shutter
CloseShutter	c	Close shutter
SelectFSR0	0	Select the first fast shift register
SelectFSR1	1	Select the second fast shift register
Polarity0	p	Set the negative polarity (electrons collection)
Polarity1	P	Set the positive polarity (holes collection)
DCShutdown	x	Turn off the power supplies of the Medipix2 device
DCStartUp	X	Turn on the power supplies of the Medipix2 device
DmaAdcConversion	a	Start the DMA[4] ADC conversion for back side pulse sampling
SetBias	b	Set the bias source output voltage
Help	h	Send the command list to the host PC
Info	i	Send the information about device (serial number, etc.)
SendSettings	n	Send the actual setting of Medipix2 CMOS inputs

Table 3.1: *List of the command services*

3.3.2 Example command – Bias voltage settings

One of the command services from the command table serves for setting the output voltage of the bias circuit. The command service subroutine is shown in Figure 3.3.

At the beginning of the subroutine, the accumulator and SPI configuration register is stored in the stack. After that, the initiating character is returned via the USB, to let the host PC know, which subroutine is executed. Because the speed of the SPI interface is at the side of MAX1932 chip limited to 2 MHz, the SPICON register must be reconfigured to match this value. The timing of the communication must follow the chip specification shown in Figure 2.8.

[4] Direct Memory Access

```
;-------------------------------------------------------------------------------------
ComServ_SetBias:
    PUSH  ACC             ; Store the accumulator to the stack
    PUSH  SPICON          ; Store the SPI configuration register to the stack

    MOV   A,#'b'          ; Store the initiating character to the accumulator
    CALL  FT_SendChar     ; Send the initiating character via USB

    MOV   SPICON,#33h     ; Configure the SPI interface
    CLR   P3.7            ; Enable the SPI inputs of MAX1932
    CALL  FT_GetChar      ; Wait for value to be written to MAX1932

    MOV   SPIDAT,A        ; Send value
    JNB   ISPI,$          ; Wait until whole byte is send via SPI to MAX1932
    CLR   ISPI            ; The SPI interrupt bit has to be cleared

    SETB  P3.7            ; Disable the SPI inputs of MAX1932

    MOV   DPTR,#Str_OK    ; Set the specified string address to the DPTR
    CALL  FT_SendString   ; Send the message via USB

    POP   SPICON          ; Restore the SPI configuration register from the stack
    POP   ACC             ; Restore the accumulator to the stack
    RET
;-------------------------------------------------------------------------------------
```

Figure 3.3: *Example of the command service – Bias voltage settings*

When the SPI interface is configured properly the P3.7 pin of the microcontroller is pulled low to enable the SPI inputs of MAX1932 device. Than the FT_GetChar routine is called to obtain the value, which has be sent to the bias circuit, from the host PC. After the byte is received it is sent via SPI. The SPI interrupt bit called ISPI signalizes the end of the transmission. After the successful transmission the P3.7 pin is set high and SPI inputs of MAX1932 is disabled and the 'OK' message is sent via the USB interface.

At the end of the subroutine the accumulator and SPI register are restored from the stack and the RET instruction is executed to jump to the WaitForCommand label of the main endless loop as it is described in chapter 3.3.1.

3.4 Host PC software for system debugging

For testing the functionality of the interface was used a simple C++ based software which allows to send the commands and receive answers from tested interface and display in graphically (see the software screenshot at Figure 3.4). This software is decided only for interface testing purposes. The final version of the host PC software will be developed as a plug-in module within the existing complex program package, which will allow measurements with both interfaces (USB and MUROS2), stepper motors controlling (sample movement, rotation...), etc. I would like to note that developing of the software for host PC is not part of my work.

Figure 4.3 below shows the screenshot of the software during its usage. At the left side of the screen are situated the buttons for Medipix2 ADC and DAC setting and shutter control. In the window in left bottom corner of the screen the data incoming from the USB interface are listed in hexadecimal and ASCII format. Here is also possible to send any character or a string of characters to the interface.

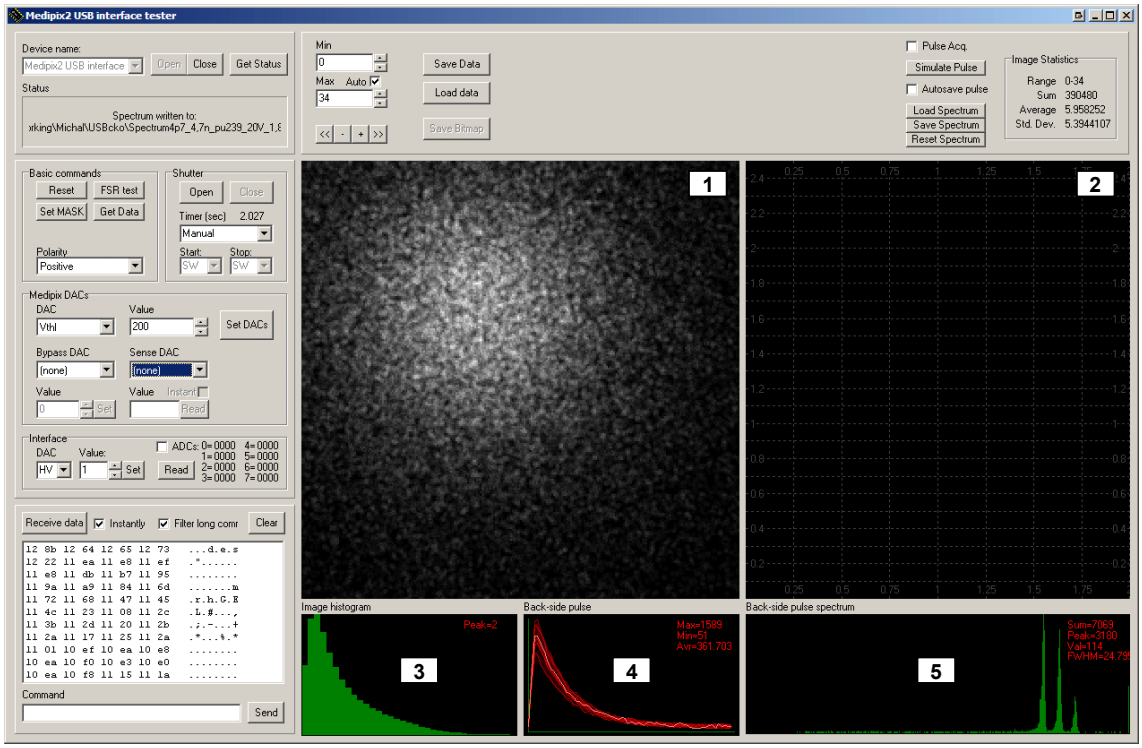


Figure 3.4: *Screenshot of the software window during the measurement*

Main part of the screen is occupied by picture windows. Window number 1 shows the measured image (read-out of the Medipix2 mask). The right upper corner of the screenshot shows some statistical data about image. In window number 2 the status of ADCs of the microcontrollers is presented. The ADC read function was turned off during the measurement, so this window is empty. The image number 3 displays the histogram of the image from the window 1. Window 4 shows the sampled waveform of back-side pulse. The maximum of the sampled pulse is detected and used for the spectrum generation in the window 5.

4 Interface Testing

In this chapter the first tests of the interface prototype based on QuickStart development kit from Analog Devices are presented. The beginning of the chapter deals with the testing of individual function blocks of the interface. The second part follows with a real measurement using an alpha particle source.

4.1 Development process

During the interface development certain problems appeared. Some blocks (Microcontroller wit ADC, high voltage source circuit) were working properly without any problems but others did not. Specific hardware problems which were discovered during the interface testing are described below.

4.1.1 USB interface

The block of USB interface based on FT245BM works fine except of the switching circuit with a MOSFET transistor. The connection of the soft start circuit according to the recommendation of the datasheet ([11], p. 20) still causes large transient power surge when the MOSFET is turning on and thus resets the FT245BM device. The connection presented in the Figure 2.2, solves this problem by using the R35 = 10 kΩ instead of recommended 1 kΩ and by placing the capacitor C37 between the gate of T1 and ground instead of between the gate and drain. The resistor R34 serves for a faster transistor turn off immediately after the USB cable gets connected.

4.1.2 Power supplies

Power supplies are the most critical part of the interface. The main problem is that the only single-sided universal PCB is used for the prototype construction, so there is no ground plate and a parasitic coupling can emerge easily. I suppose that the final four layers PCB (in fabrication) will significantly improve stability of the power supplies.

As the maximal output current of the microcontroller for the high logic level is 80 µA (larger output current causes drop of the output voltage below 4 V) the value of the resistor R49 to base of T2 (see Figure 2.10) must be at least ten times larger than recommended value at MAX1951 datasheet ([17], p. 12). This value is still sufficient for proper function of the transistor.

4.1.3 Logical levels conversion

The presence of three different TTL/CMOS logics in the circuit complicates the design because several logic levels converters must be used (also footprints of parts have to be considered due to PCB dimensions). Various possible solutions shown at Figure 4.1 were tested (resistor divider, divider with Schottky diode, transistor switch).

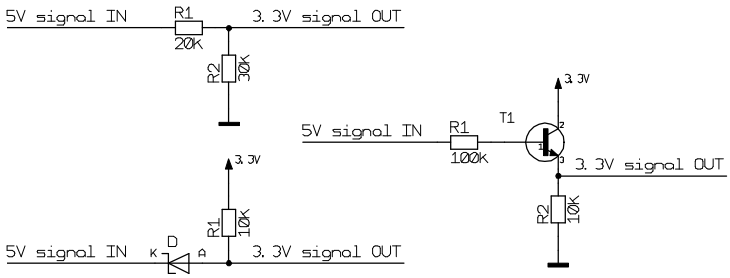


Figure 4.1: *Logic levels conversions*

Performance of all such converters was poor (large current consumption or pulse shape deformation). Finally, the best results were reached by utilizing circuits from the 74LCXxxx low voltage family with 5 V tolerant inputs. This solution also saves the place on PCB.

4.1.4 Medipix2 communication

When the problems with power supplies and logical levels conversion were solved the test of the serial communication with the Medipix2 device was done. The test procedure consists of setting a Medipix2 configuration matrix followed by matrix readout. The read matrix has to be the same as the sent one.

The data from the Medipix2 device are received as a sequence of 8-bit bursts. In the first step the SPI interface is configured to receive one byte. Thus it generates eight *SCLK* pulses and receives eight bits of data. Then the CPU[1] puts received byte to the output FIFO of the FT245BM device which will send it to the host PC.

The transfer of each byte from Medipix2 to the host PC takes 2.88 µs (with 11.0592 MHz crystal), so the whole matrix consisting of 114689 bytes is transmitted in 330 ms. In the final version of interface the 20 MHz crystal will be used so the expected matrix read-out speed is about six frames per second. The Figure 4.2 shows the waveform of serial communication from oscilloscope.

[1] Central Processing Unit

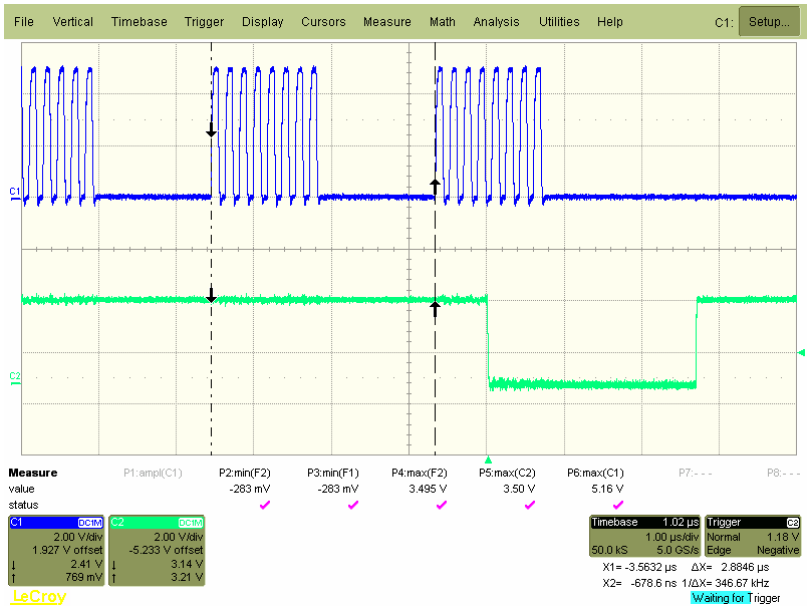


Figure 4.2: *Medipix2 serial communication (SCLK – top, ENABLE_OUT – bottom)*

4.1.5 Detector bias

The quality of detector bias has significant influence on the noise characteristic of pixels and on the whole detector performance. If the spectrometric properties of the detector are required (see the back-side pulse spectrometry configuration in Figure 4.6) the HV[2] source for detector bias has to be as stable as possible. The following Figure 4.3 and Figure 4.4 shows the output ripple and noise distribution of the high voltage supply operating at 20 V with current of 0.9 mA.

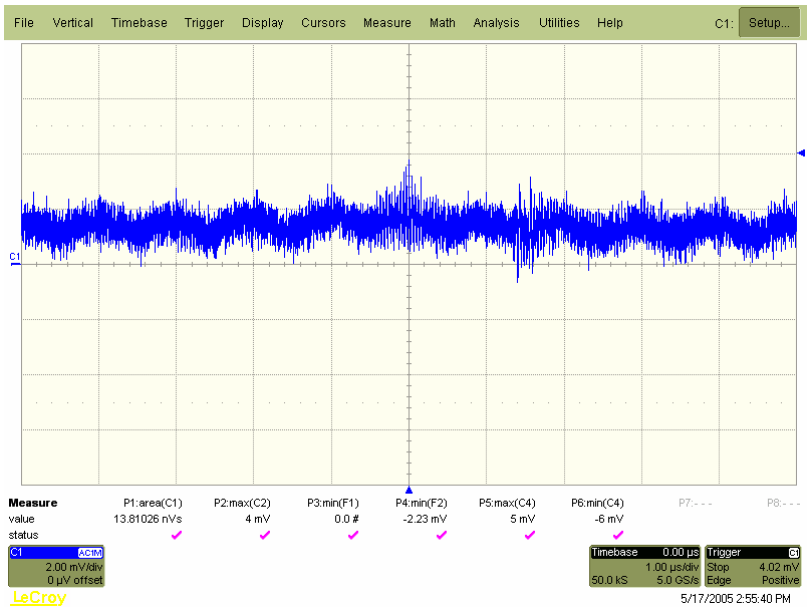


Figure 4.3: *Bias voltage noise (AC coupling, 2 mV/div, I = 0.9 mA)*

[2] High Voltage

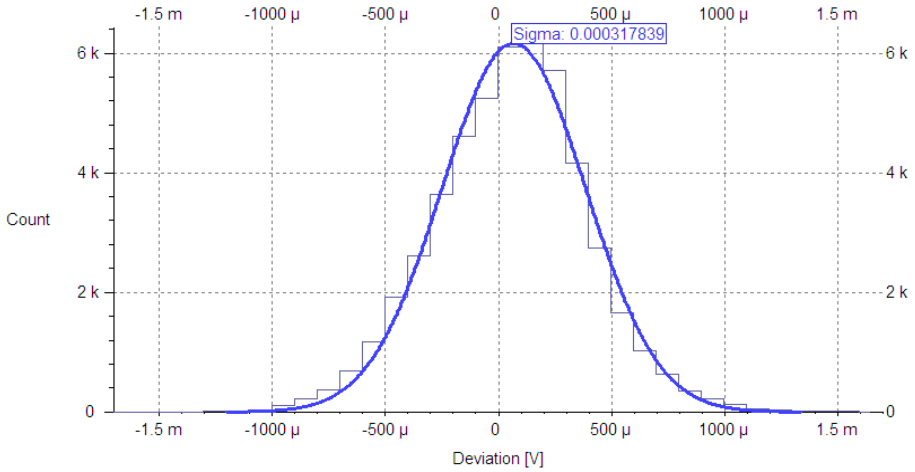


Figure 4.4: *Bias voltage noise distribution (20 V, 0.9 mA)*

The output noise is independent of the output voltage as documented by measurement presented in Table 4.1. It shows the detector bias noise characteristics as a function of output voltages.

Output voltage	Peak to peak	RMSE[3]
20 V	4,6 mV	0,34 mV
40 V	3,7 mV	0,38 mV
60 V	4,3 mV	0,35 mV
90 V	3,4 mV	0,32 mV

Table 4.1: *Bias voltage noise at different output voltages*

4.2 Testing measurement

For the interface testing was used a mixed alpha source composed of ^{239}Pu, ^{241}Am a ^{244}Cm. The list of alpha particles energies emitted by this source is shown in Table 4.2.

Element	Peak number	1	2	3
^{239}Pu	Peak energy	5,1534 MeV	5,1046 MeV	---
	Relative intensity	88,4 %	11,5 %	---
^{241}Am	Peak energy	5,4857 MeV	5,4429 MeV	5,389 MeV
	Relative intensity	86 %	12,7 %	1,3 %
^{244}Cm	Peak energy	5,8049 MeV	5,7629 MeV	---
	Relative intensity	76,6 %	23,3 %	---

Table 4.2: *Energetic spectrum of mixed alpha source*

[3] Root Mean Square Error

4.2.1 Sample picture measured with new interface

The measurement with the interface prototype was performed at following conditions:

- Alpha source to Medipix2 distance: 5 mm (in air)
- Time of measurement: 2 min
- Bias voltage: 60 V
- Medipix2 DAC settings: V_{thL} = 250, V_{thH} = 0, V_{fbk} = 200, other DACs had default values

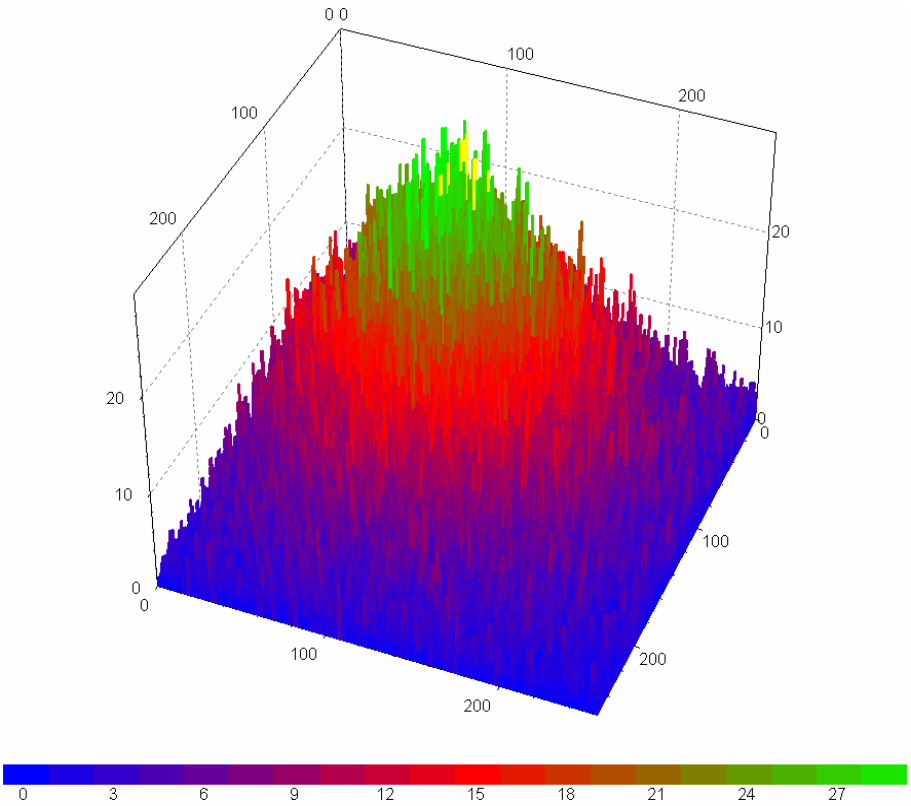


Figure 4.5: *Planar profile of measured mixed alpha source*

The measured picture is shown in Figure 4.5 (see also the print screen of the PC software window during the measurement in Figure 3.4).

4.2.2 Back-side pulse spectrometry

The charge collected after the interaction of the ionizing particle creates a current pulse. The pulse goes not only through the interacting pixel, but also through the bias high voltage source. This makes possible to monitor this pulse in the HV circuit and allows obtaining spectroscopic information about energy of each particle interacting in the detector sensor (see Figure 4.6).

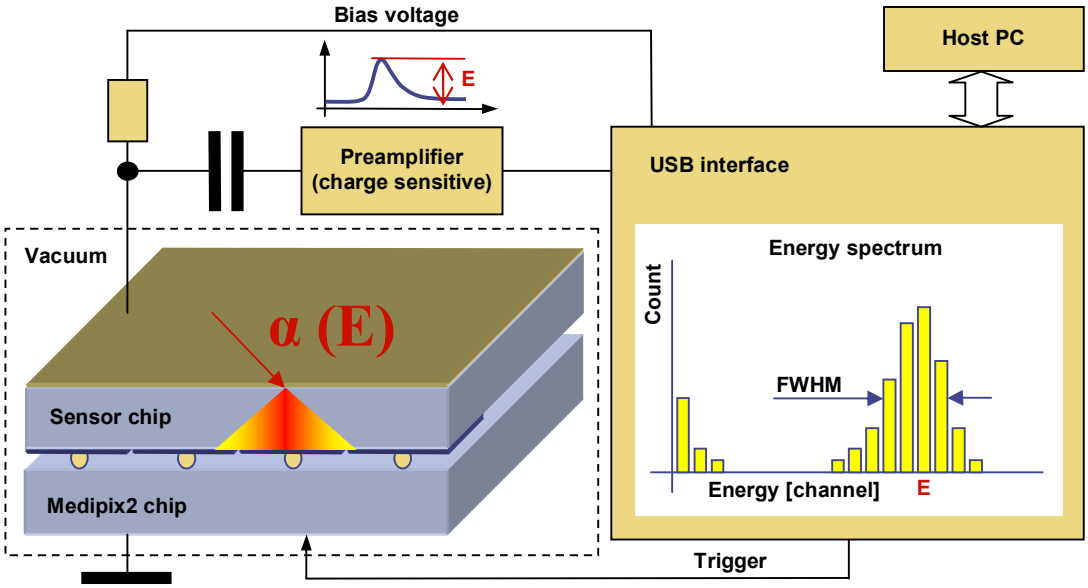


Figure 4.6: *Experimental setup for back-side pulse spectrometry*

The noise in the back-side pulse is superposition of the noise from each pixel. As the whole detector area is much bigger than the pixel size, the expected energy resolution of such spectrometer will not be comparable to standard spectroscopic Si-diodes. Nevertheless, it should be sufficient for spectrometry of heavy charged particles thanks to their large energies. The back-side pulse can be also used for the triggering and counting of interacting particles.

With the experimental setup depicted in the Figure 4.6 and the alpha source described above a testing measurement was done under following conditions:

- Alpha source to Medipix2 distance: 20 mm (in vacuum 50 Pa);
- Time of measurement: 2 min;
- Bias voltage: 90 V (provided by the integrated HV source);
- Preamplifier PEVOT;
- Amplifier from the spectroscopic system CICERO[4];
- Medipix2 DAC settings: VthL = 250, VthH = 0, Vfbk = 200, other DACs has default values;

The alpha spectrum measured independently with the developed prototype of the USB interface and with commercial multichannel analyzer CICERO is shown in following figures.

[4] CICERO - 8k multichannel analyzer by SILENA Milano

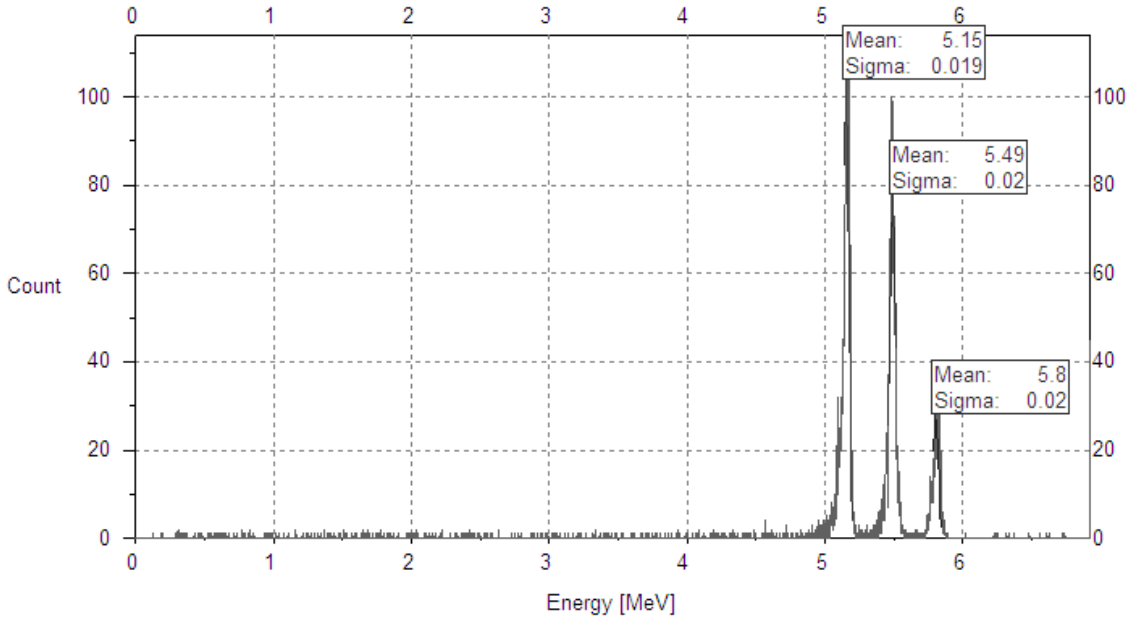


Figure 4.7: *Spectrum of mixed α-source measured by the developed USB interface*

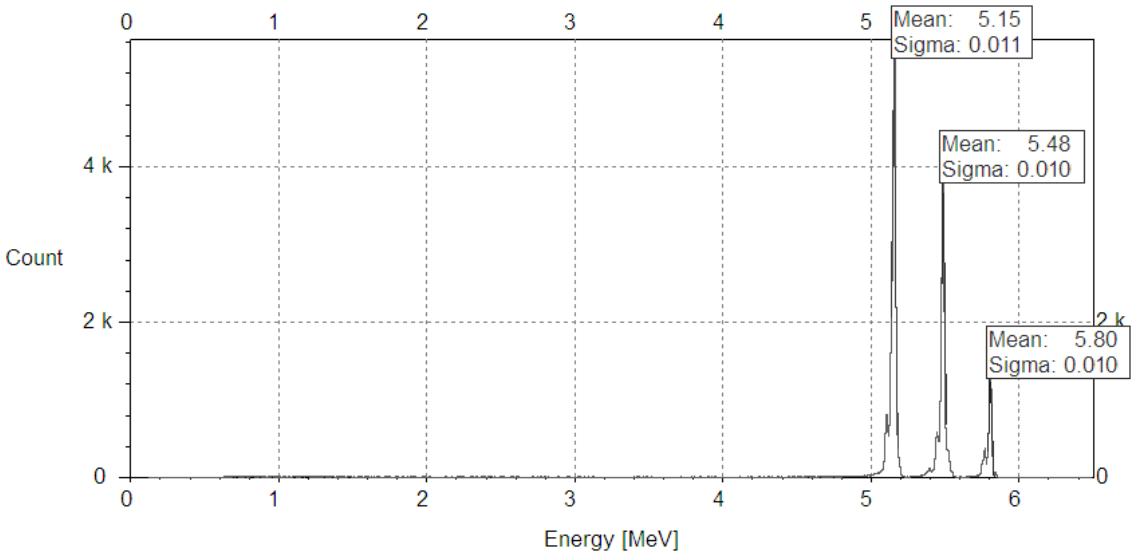


Figure 4.8: *Spectrum of mixed α-source measured by CICERO analyzer*

The energy resolution of the back-side pulse spectrometry with Medipix2 and USB interface is about 44 keV in terms of FWHM (Full Width at Half Maximum). The energy resolution measured by specialized spectrometric system CICERO at the same conditions is 23 keV. With respect to the level of miniaturization used in USB interface this is a satisfactory result and can be improved by better processing of the sampled data (currently just the sampled pulse maximum is used for the spectrum generation).

Conclusion

The principle of the position sensitive semiconductor detectors is given in chapter 1. In this chapter is also described the hybrid semiconductor pixel detector Medipix2 with consideration to restrictions given by the present chipboard.

The readout system for Medipix2 pixel detector based on the USB interface was developed to improve the system portability and spectrum of usage (spectroscopic applications). The new interface enables full control of the Medipix2 chip and integrates all necessary support circuits into one small PCB (60 x 45 mm^2). All power supplies including the detector bias one (up to 90 V) are internally derived from the voltage provided by the USB connection. The whole interface is controlled by microprocessor what gives a high level of flexibility.

One of the most significant advantages is the support of back-side pulse processing. The charge generated by an ionizing particle is measured in bias circuit and can be used for spectroscopy or triggering. With the present design the energy resolution of such spectrometer is about 44 keV for 5.5 MeV alpha particles (see Figure 4.7). The quality of measured spectra highly depends on the noise characteristics of the bias voltage source. The comparison of the spectra measured with USB interface (see Figure 4.7, FWHM = 44 keV) and the spectra obtained from the commercial multichannel analyzer CICERO (see Figure 4.8, FWHM = 23 keV) shows that quality of the integrated high voltage source is sufficient. The resolution can be improved by better processing of the sampled data.

The back-side pulse feature also allows monitoring the number of interacting heavy charge particles, so that the Medipix2 device can be read-out when the required number of hits is reached. It can help to optimize the amount of transferred data.

The general features of the new interface can be summarized to following points:

- Readout speed is 6 frames per second.
- Source of variable detector bias with leakage current monitor is integrated.
- Internal analog and digital interface for "plug-in" PCB modules connection. The modules can be used for the shielded analog circuits as charge sensitive preamplifier for back-side pulse processing, for additional memory modules, for stepper motor control, for trigger generator, etc.
- 8x 12-bit fast ADC. Two channels are used for the detector bias voltage and current monitoring. One can serve for calibration of the Medipix2 internal DACs. Others can be used by plug-in PCB modules.
- 2x DAC. One channel is devoted to the bypass one of the Medipix2 internal DACs. Second is used for the test pulse generation. When these features are not needed both DACs can be redirected to the plug-in module interface.
- Advanced triggering. The acquisition can be started by host PC or external trigger signal and stopped by host PC, external trigger and internal timer/counter. All start-stop option combinations are possible.

- Hardware timer precisely measures the time of the data acquisition and can be used to stop the measurement after preset time period.
- Trigger output to notify the end of the acquisition to the other devices (stepper motor, X-ray tube controlling...)
- 4kB EEPROM for interface configuration + 128kB of optional EEPROM for chip configuration.
- Temperature monitoring.
- Ability to control other devices via I^2C bus.
- Ability to flash a firmware (via special cable and serial interface).

Above mentioned features were tested on the interface prototype based on QuickStart development kit from Analog Devices. The production of the final PCB is in progress and the Medipix2 device with the USB readout is expected to be fully operational at the time of thesis defence.

Acknowledgements

I would like to express my extensive gratitude to my supervisor Ing. Jan Jakůbek, Ph.D., who proposed the subject of this thesis and kindly led the development of the interface to its successful end. I would also like to mention my consultants Ing. Vladimír Linhart and Dr. Ing. Milan Šiňor and all the people from the Medipix2 collaboration. They were kind and helpful enough. My special thanks go to Ing. Stanislav Pospíšil DrSc., the director of the Institute of Experimental and Applied Physics for the possibility of access to the institute experimental equipment and last but not least for the financial support of the institute[5].

[5] Project MŠMT 1P04LA211 "Spolupráce ČR s CERN", subproject Medipix

List of Figures

List of Tables

Abbreviation List

AC - Alternating Current
ADC - Analog to Digital Converter
ASCII - American Standard Code for Information Interchange
ASIC - Application Specific Integrated Circuit
CCD - Charge Coupled Device
CERN - Centre Europeen pour Recherche Nucleare
CMOS - Complementary Metal Oxide Semiconductor
CPU - Central Processing Unit
CST - Charge Sharing Test
DAC - Digital to Analog Converter
DC - Direct Current
DDL - Double Discriminator Logic
DMA - Direct Memory Access
EEPROM - Electrically Erasable Programmable Read Only Memory
ESR - Equivalent Serial Resistance
FIFO - First In First Out
FPGA - Field Programmable Gate Array
FSR - Fast Shift Register
FWHM - Full Width at Half Maximum
HV - High Voltage
I^2C - Internal Integrated Circuit
IDE - Integrated Development Environment
LHC - Large Hadron Collider
LSB - Least Significant Bit
LVCMOS - Low Voltage Complementary Metal Oxide Semiconductor
LVDS - Low Voltage Differential Signaling
LVTTL - Low Voltage Transistor Transistor Logic
MCU - Micro Controller Unit
Medipix2 - MEDical Imaging PIXel detector 2nd generation
MIPS - Million Instructions Per Second
MOSFET - Metal Oxide Semiconductor Field Effect Transistor
MSB - Most Significant Bit
MUROS2 - Medipix2 re-Usable Read-Out System version 2
PC - Personal Computer
PCB - Printed Circuit board
PCI - Personal Computer Interconnect
PCI - Personal Computer Interconnected
PID - Product identification
PnP - Plug & Play
PWM - Pulse Width Modulation
RMSE - Root Mean Square Error
SOI - Silicon On Insulator
SPI - Serial Peripheral Interface
TTL - Transistor Transistor Logic

UART - Universal Asynchronous Receiver/Transmitter
USB - Universal Serial Bus
VHDCI - Very High Density Cable Interconnect
VID - Vendor Identification
WASP - Windows Analog Software Program
WSD - Windows Serial Downloader

Bibliography

[1] Medipix collaboration homepage at: http://www.cern.ch/medipix

[2] J. Gerndt, *Detektory ionizujícího záření*, ČVUT v Praze, 1996

[3] B. Mikulec, *Single Photon Detection with Semiconductor Pixel Arrays for Medical Imaging Applications*, PhD Thesis, University of Vienna, June 2000

[4] X. Llopart, M. Campbell, R. Dinapoli, D. San Segundo and E. Pernigotti, *Medipix2, a 64k pixel readout chip with 55 μm square elements working in single photon counting mode*, IEEE Trans. Nucl. Sci., vol. 49, 2279-2283, October 2002

[5] C. Schwarz, M. Campbell, R. Goeppert, E.H.M. Heijne, J. Ludwig, G.Meddeler, B. Mikulec, E. Pernigotti, M. Rogalla, K. Runge, A. Söldner-Rembold, K.M. Smith, W. Snoeys, J. Watt, *X-ray imaging using a hybrid photon counting GaAs pixel detector*, Nucl.Physics B (Proc.Suppl.) 78 (1999) 491-496

[6] E. Belau et al., *Silicon detectors with 5 μm spatial resolution for high energy particles*, Nucl. Instr. and Meth. A 217 (1983) 224-228

[7] Z. Vykydal, *Automatizace ve spektrometrické laboratoři a popis spektrometru JAK*, Výzkumný úkol, ČVUT v Praze, 2003

User's manuals:

[8] *8051 Cross Assembler User's Manual*, MetaLink Corporation P.O. BOX 1329 Chandler, Arizona 85244-1329

[9] X. Llopart, *Medipix2 User's Manual*, CERN, distributed only between members of the Medipix Collaboration

[10] D.S.S. Bello, *MUROS2 User's Manual*, NIKHEF Amsterdam, July 2003 edition, distributed only between members of the Medipix Collaboration

Component datasheets:

[11] FT245BM - USB – Parallel FIFO datasheet at: http://www.ftdichip.com/Documents/DataSheets/ds245b16.pdf

[12] ADuC841 Precision Analog Microcontroller datasheet at: http://www.analog.com/UploadedFiles/Data_Sheets/2479059961574193522626 70829ADuC841_2_3_0.pdf

[13] MAX9122 Quad LVDS Line Receivers with Integrated Termination datasheet at: http://pdfserv.maxim-ic.com/en/ds/MAX9121-MAX9122.pdf

[14] MAX9123 Quad LVDS Line Driver datasheet at: http://pdfserv.maxim-ic.com/en/ds/MAX9123.pdf

[15] 74LCX244 Low Voltage Buffer/Line Driver datasheet at: http://www.fairchildsemi.com/ds/74/74LCX244.pdf

[16] 74LCX573 Low Voltage Octal Latch datasheet at: http://www.fairchildsemi.com/ds/74/74LCX573.pdf

[17] MAX1951 2A PWM step-down DC-to-DC regulator datasheet at: http://pdfserv.maxim-ic.com/en/ds/MAX1951-MAX1952.pdf

[18] MAX1932 - Digitally Controlled, 0.5% Accurate Bias Supply datasheet at: http://pdfserv.maxim-ic.com/en/ds/MAX1932.pdf

Technical notes and specifications:

[19] Application Note AN10156, *Sorting through the low voltage logic maze* at: http://www.standardics.philips.com/support/appnotes/logic/pdf/an10156.pdf

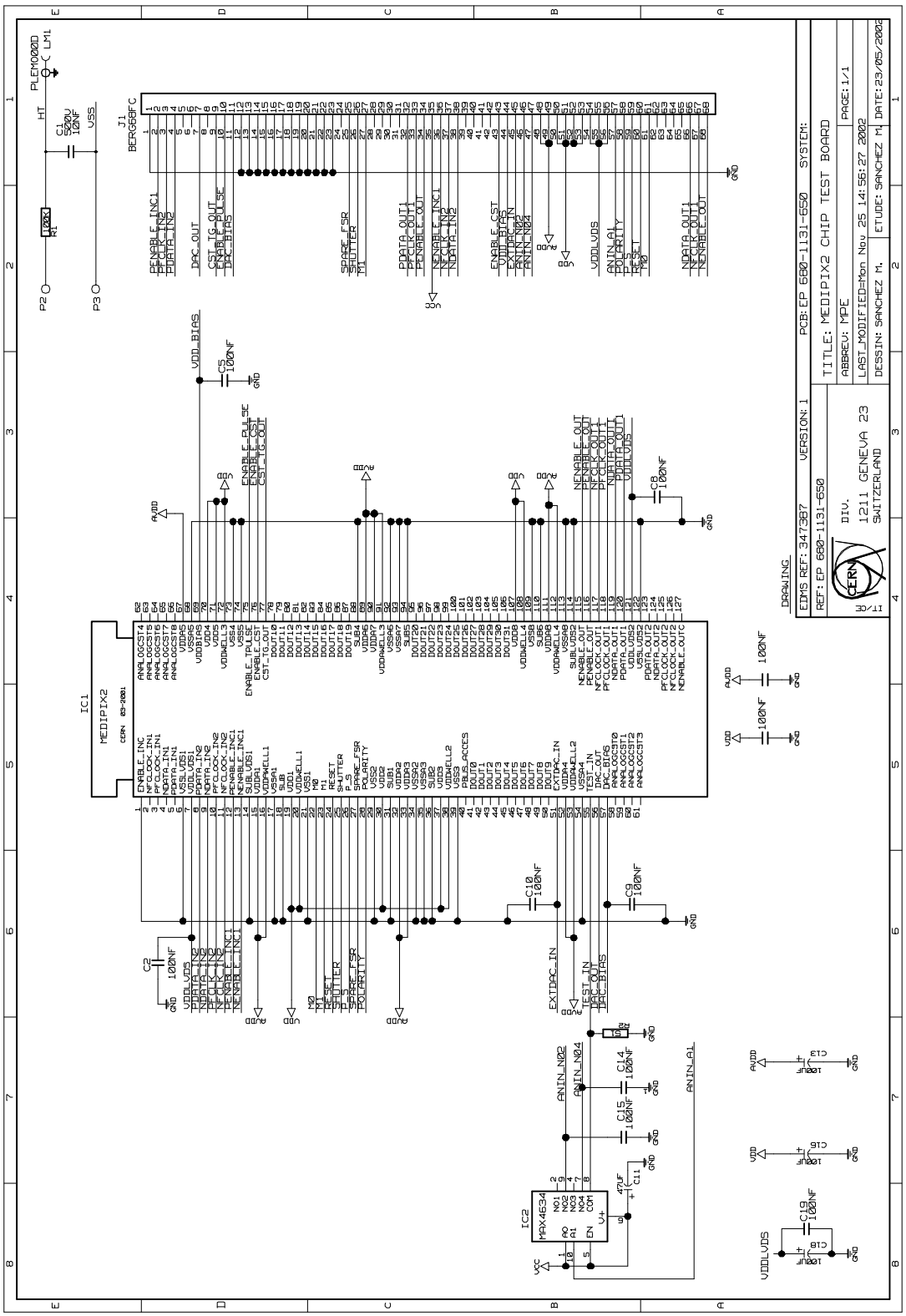
[20] Technical Note - uC004, *Understanding the Serial Download Protocol* at: http://www.analog.com/UploadedFiles/Application_Notes/1725421uC004_v30.pdf

[21] Technical Note - uC006, *A 4-wire UART-to-PC Interface* at: http://www.analog.com/UploadedFiles/Application_Notes/41642879333297uC006___A_4_wire_UART_to_PC_Interface.pdf

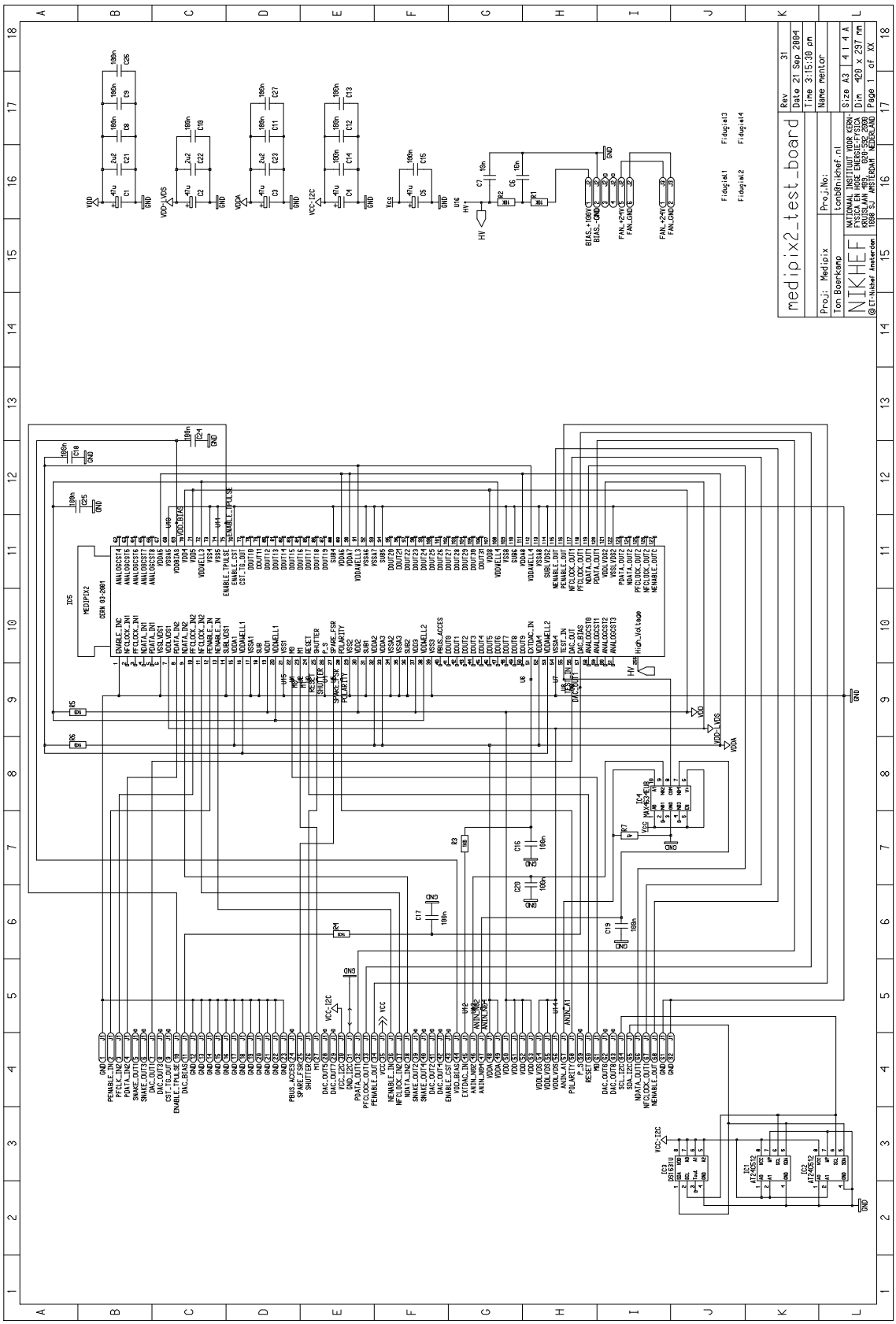
[22] Universal Serial Bus specification at: http://www.usb.org/developers/docs/usbspec.zip

[23] MProg 2.3 – FTDI EEPROM Programming Utility at: http://www.ftdichip.com/Resources/Utilities/MProg230_Setup.zip

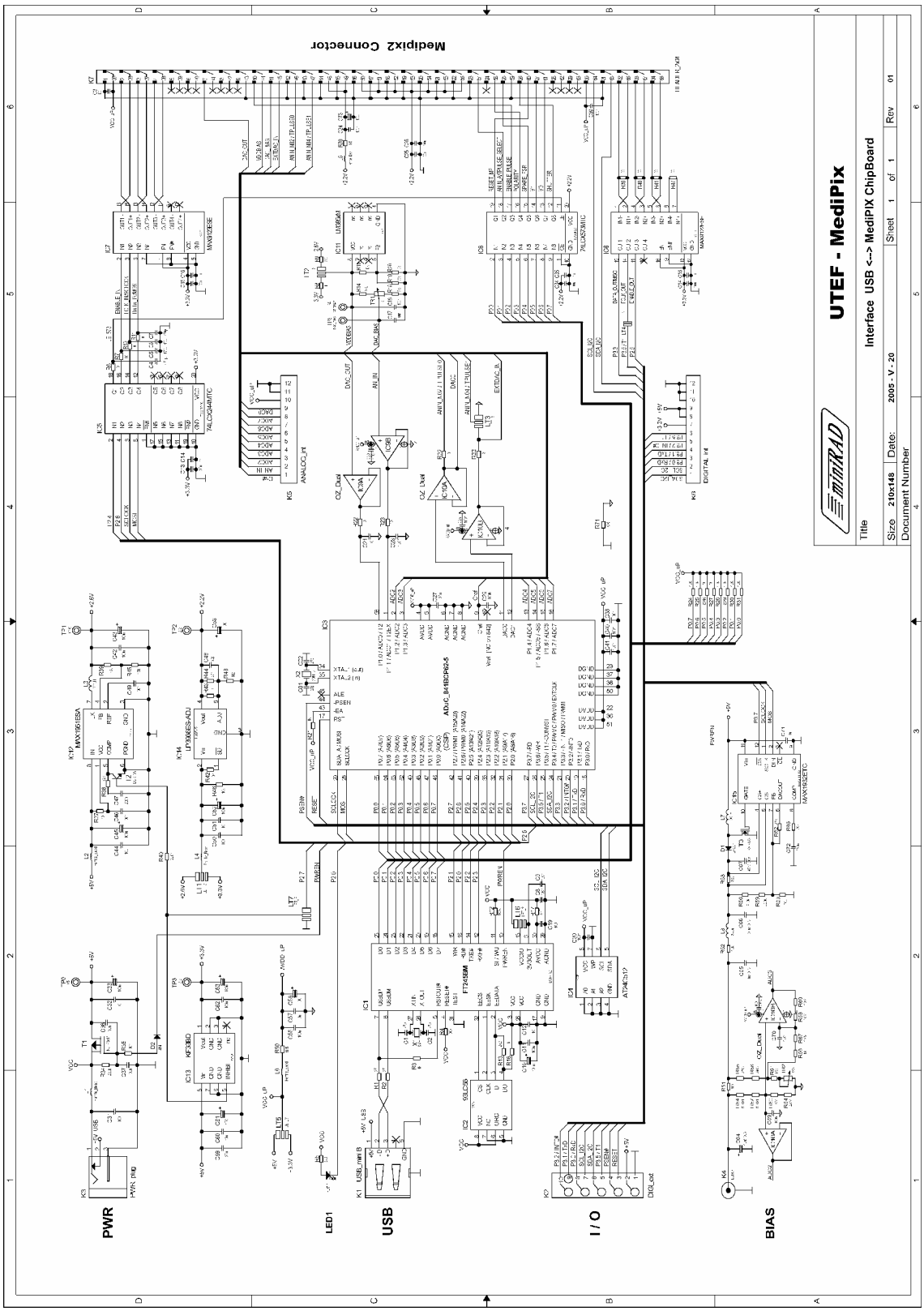
Appendix A – Wiring Diagrams



Appendix A.1: *Diagram of the standard chipboard*

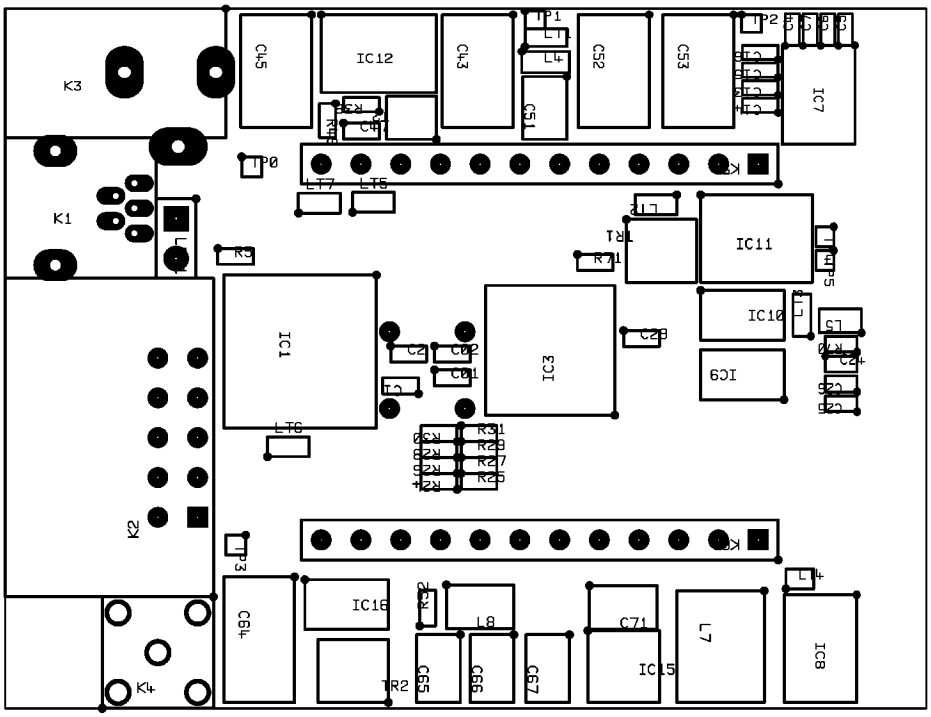


Appendix A.2: *A new chipboard schematic*

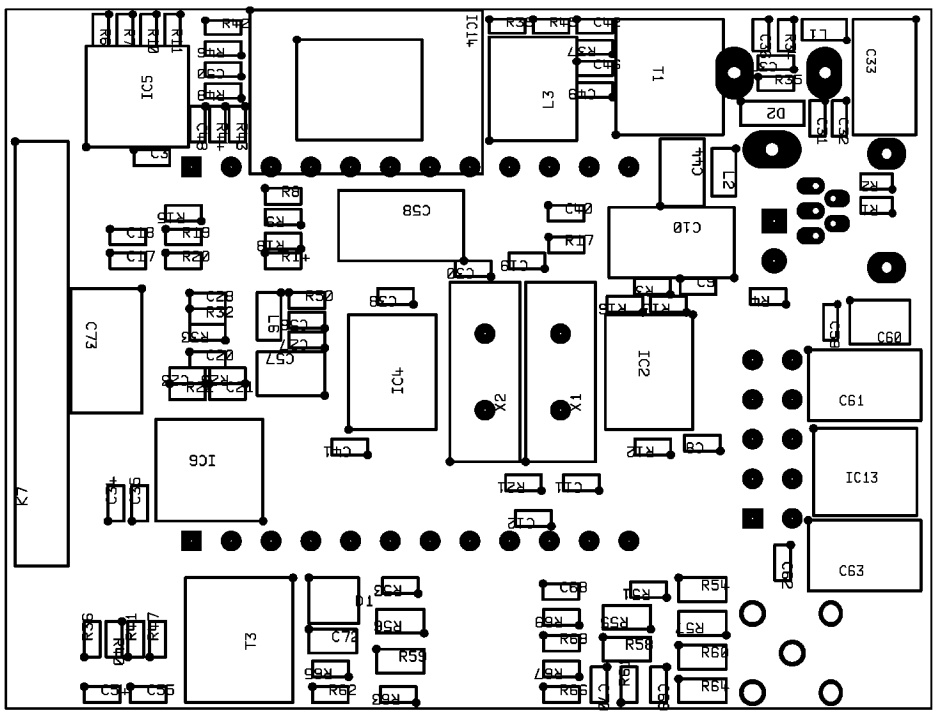


Appendix A.3: *The Medipix2 USB read-out interface diagram*

Appendix B – PCB Layout Diagrams

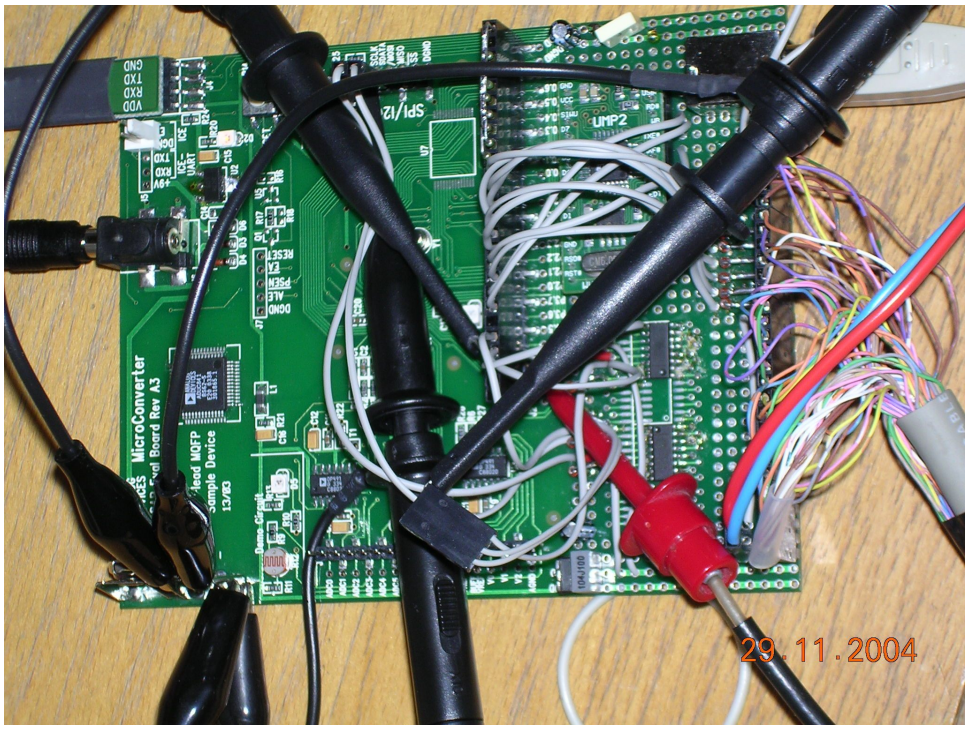


Appendix B.1: *Layout of the Medipix2 USB read-out interface (top view)*

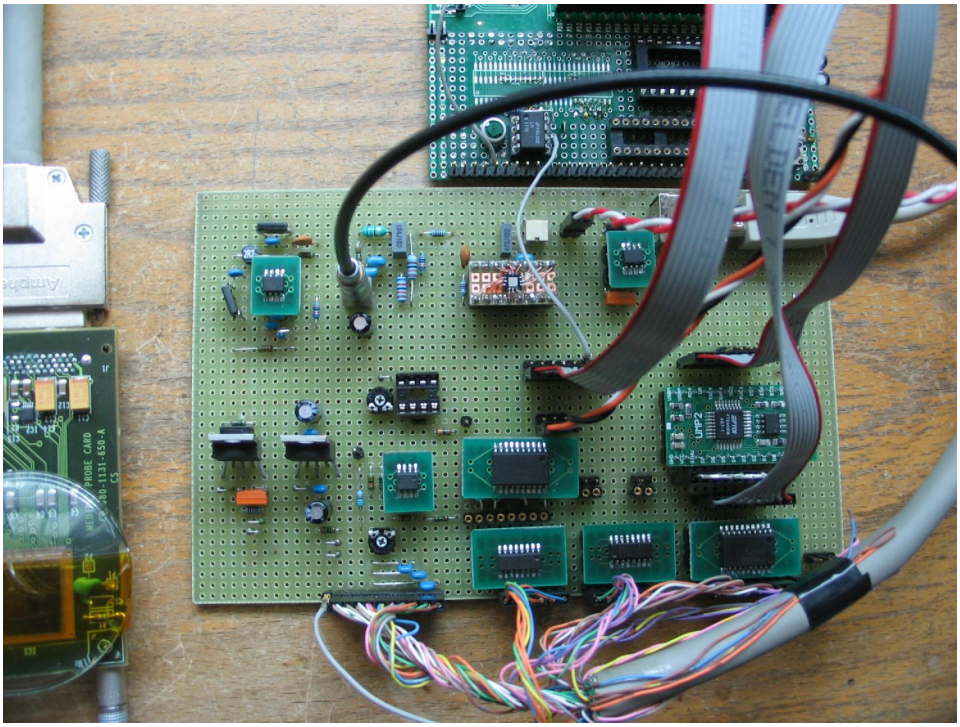


Appendix B.2: *Layout of the Medipix2 USB read-out interface (bottom view)*

Appendix C – Prototype Photos



Appendix C.1: *First version of the prototype*



Appendix C.2: *Second version of the prototype*